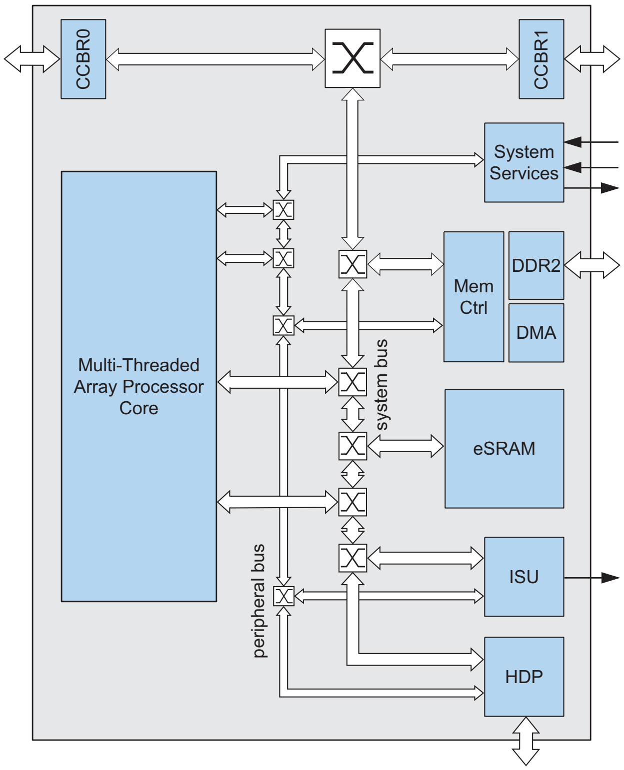
ClearSpeed™

CSX600 Datasheet

Advanced Product Data



Description

The CSX600 is a high performance, low power floating point coprocessor. It is designed for use in a variety of applications in high performance computing and embedded systems.

The CSX600 is the first product in ClearSpeed's family of floating point application accelerators. The CSX processors are based around ClearSpeed's multi-threaded array processor (MTAP) architecture. This architecture has been developed to address the implementation issues of high-performance systems by providing unparalleled performance-per-watt.

High performance

- 25 GFLOPS sustained
- 250 MHz core clock
- Power efficient architecture

Features

- Professional Software Development Kit (SDK)
- 128 Kbyte on-chip SRAM
- Supports up to 8 Gbytes of DDR2 DRAM
- 8 Kbyte instruction and 4 Kbyte data caches
- Array of 96 Processing Elements
- FPU acceleration on every PE
- Two high speed data ports.
- Dedicated host interface port
- JTAG boundary scan

Applications

Designed for data-intensive and high-compute applications

- Network processing
- Radar systems
- Bio-informatics
- Signal processing
- Medical imaging

Electrical

- 1.2V core supply
- 1.8V I/O pad supplies
- 1.5V analog supplies

Mechanical/thermal

- 35 mm x 35 mm thermally enhanced flip-chip BGA package
- 1,011 balls on 1 mm pitch
- 433 signal pins (including analog supplies)

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PRELIMINARY TECHNICAL DATA

Overview

The CSX600 comprises a multi-threaded array processor (MTAP) core, external DRAM interface, high-speed interfaces and embedded SRAM integrated onto a single chip. All subsystems on the chip are interconnected via the ClearConnect on-chip network.

Processor core

The MTAP architecture provides an exceptionally powerful and scalable processing solution, based on an array of tens to thousands of Processing Elements (PEs). Each PE has its own local memory and I/O capability, making the architecture ideally suited for applications which have high processing and/or bandwidth requirements. The inherently scalable array architecture is also highly area and power efficient.

The MTAP core contains an array of 96 Processing Elements (PEs). The PEs include multiple processing units and have high level of internal instruction-level and data parallelism. Each PE also has its own local memory providing a high bandwidth access to frequently used data.

Memory hierarchy

The CSX processor has a hierarchical memory system consisting of: register files, PE memory, caches, on-chip memory and external DRAM.

External memory is connected via a 64-bit DDR2 DRAM interface. When used with a 72-bit wide DRAM array this provides Error Checking and Correction (ECC). Each processor supports up to 8 Gbytes of local DRAM.

The processor supports 64-bit addressing so that large data sets can be processed. The 64-bit address space is flexibly mapped into a 48-bit physical address space distributed across multiple processors. For embedded systems and backward compatibility a simple 32-bit addressing mode is provided.

On-chip SRAM is included for frequently accessed code and data.

The on-chip DMA controller can be programmed to transfer data to and from the external memory interface and any other device on the ClearConnect bus.

ClearConnect bus

The ClearConnect bus used as the interconnect on the CSX600 is a packet switched on-chip network that provides high bandwidth and low power consumption. It supports multiple concurrent transfers, thus providing extremely high aggregate bandwidth. The bus is also used, via the bridge ports described below, to provide communication between CSX processors using a consistent protocol and addressing scheme.

Host interface and debug port (HDP)

The HDP is the means by which the CSX600 is configured, booted and controlled by a host processor. It carries master and slave transactions in both directions, and has full access to the register and memory space of the device.

The external interface uses a low pin-count interface that is optimized to allow a host to have low-cost access to a number of CSX600 devices on a board.

Interrupt & semaphore unit (ISU)

The Interrupt and Semaphore Unit supports the synchronization between threads and with external events. Multiple processors may perform synchronization events, for example to assist in communication via shared memory, through operations on the set of hardware semaphore elements contained in this block. Similarly, synchronization with a host processor may be performed via conversion of semaphore events to interrupt events. Both pin and message-signalled interrupts are supported for flexible support of multiple devices in various host environments.

ClearConnect bridge ports (CCBR)

The internal bus is made available at two ports which can be interconnected with no glue logic to construct multiprocessor systems. This enables system performance to be scaled to meet the requirements of the application. Data can be routed directly from one bridge port to the other without impacting on any other internal bus traffic.

These ports use double data rate interfaces to minimize the pin count. If not fully used, they can be selectively turned off to reduce power consumption.

PRELIMINARY TECHNICAL DATA

Architecture

The CSX600 integrates a multi-threaded array processor (MTAP) core, on-chip SRAM, a DDR2 DRAM interface, a host/debug port and chip-to-chip bridge ports.

Processor core

The processor core is shown in the block diagram (Figure 1). The processor consists of a control unit, a “mono” (scalar) execution unit, a “poly” (data parallel) execution unit and an I/O subsystem.

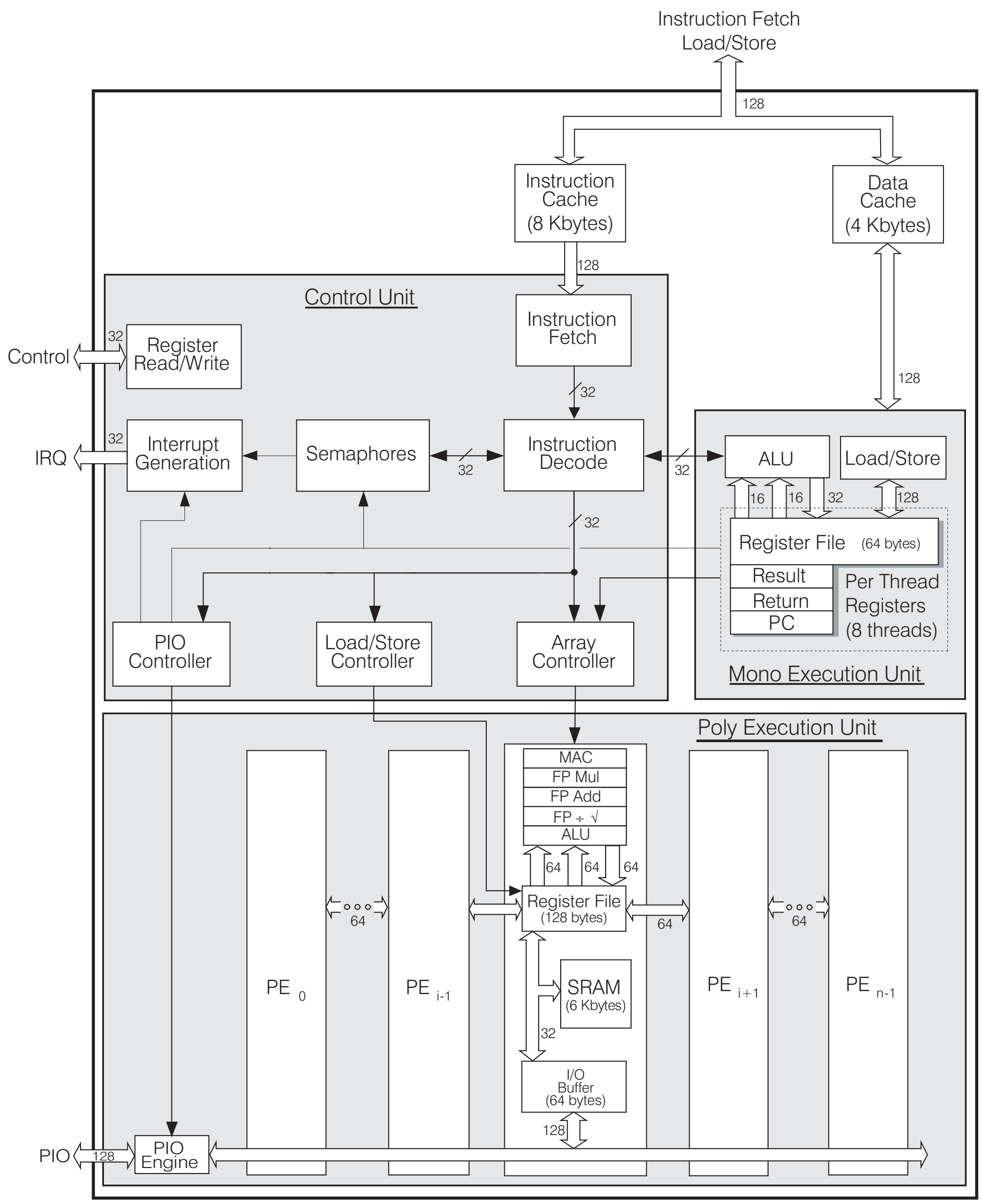

Figure 1 Processor core block diagram

This information applies to a product under development. Specifications and characteristics are subject to change without notice.

The main components of the processor are:

Execution units:

This consists of two main parts:

- The *mono* execution unit which acts on mono (non-parallel) data and handles program flow control and I/O functions;
- The *poly* execution unit which contains an array of Processing Elements (PEs) which act on poly (parallel) data.

Control unit: fetches and decodes instructions. The single, unified instruction stream fetched and decoded by the control unit. Mono instructions are despatched to the mono execution unit, poly instructions are sent to the poly execution unit;

Caches: instruction and data caches to speed accesses to external code and data;

I/O: as well as loads and stores from the mono and poly execution units, there is a *Programmed I/O* (PIO) mechanisms which allows the poly execution unit to do loads and stores to external memory.

It is the poly execution unit and its array of PEs that provide the processor's massive processing power and memory bandwidth. The mono and poly execution units have basically the same architecture and instruction set. The tightly integrated mono and poly execution units mean that the processor as a whole is efficient for simple sequential code, as well as when processing large amounts of data in parallel.

The various functional units within the execution units (e.g. ALU, FPU, I/O, etc.) can operate concurrently.

Control unit

The instruction fetch and issue hardware supports multi-threaded execution. Thread switching is under software control and may be triggered in response to events such as the completion of an operation by one of the I/O engines. By providing support in hardware, the need for a real-time kernel for the MTAP processor is removed. The hardware supports 8 threads; hardware semaphores are used to synchronize threads with other threads and with hardware units.

To optimize performance, the processor includes instruction and data caches.

Features

- Hardware support for 8 threads;
- 128 8-bit semaphores;
- Unified 32-bit instruction set;
- 8 Kbyte instruction cache, 4-way, 512 lines x 4 instructions, with manual and auto pre-fetching (configurable horizon);
- 4 Kbyte data cache, 4-way, 256 lines x 16 bytes;
- Interrupt generation;
- Debug support;
- Event counters for PAPI profiling support.

Mono execution unit

As well as handling mono data, the mono unit is responsible for program flow control (branching), thread switching and other control functions. The mono execution unit also has overall control of I/O operations. Results from these operations are returned to a register in the mono unit. The mono execution unit contains:

- ALU
- 64-bit FPU
- Multiple 128-byte register files

Poly execution unit

The processor core contains an array of 96 PEs. The array provides both compute power and high bandwidth storage. The PE array operates on a Single-Instruction Multiple-Data (SIMD) model, processing multiple data items in parallel.

Each PE contains:

- 128-byte PE register file;
- 6 Kbytes of PE SRAM;
- 16-bit MAC with 64-bit accumulator;
- Single and double precision Floating Point Unit (FPU), with dual issue pipelined add and multiply;
- Support for integer and floating point divide and square root.

Input-output

The MTAP processor supports a Programmed I/O (PIO) channel designed for transferring variable amounts and types of data under software control. This is typically used to access external memory or peripherals.

- 128-bit PIO data channel;
- Transfer sizes of 8, 16, 32, 64 bytes per PE;
- Addressing modes: addresses and strided;
- Synchronized via semaphores.

ClearConnect bus

The ClearConnect bus is a packet switched on-chip network; on the CSX600 it is configured as two independent channels. One of these is the main system bus, designed for high bandwidth data movements, the other is a peripheral bus, designed for read/write access to control registers and interrupt messages. Both system bus and peripheral bus are pipelined and split transaction for maximum performance.

The system bus runs at core clock speed, is 128 bits wide and can transfer up to 128 bytes in a single transaction. The peripheral bus is 32 bits wide and can transfer 4 bytes in each transaction.

By means of the two Bridge Ports described below, the ClearConnect bus can be extended across multiple CSX600 devices and to system logic implemented in other devices such as FPGAs. All memory targets are then accessible by all masters on the global bus, using a 48-bit physical address. Master and target units are uniquely identified by means of device IDs that are assigned to individual devices at boot time, and internal node IDs that are fixed. The combination of device & node ID forms a geographic bus address that is unique to each unit. Part of the master's logical address is used, by means of a programmable address aperture unit, to map logical addresses to physical addresses that reside on particular bus targets.

Interrupt and semaphore unit

The ISU contains three inter-related sub units. A Global Semaphore Unit (GSU) contains 32 hardware semaphores that are accessible by processor cores in order to perform coherent inter-processor communications. Semaphore operations may be explicitly added to software to synchronize the working of different processors across the inter-chip network. These inter-processor global semaphore operations are an extension of the thread-to-thread hardware semaphores, allowing the multi-threaded model to be applied to numerous CSX600 devices working in cooperation.

The Interrupt Unit (IU) and Interrupt Generator (IG) sub-units collect, mask and format interrupts from various sources in the device, including event notification from the processor core, exception conditions from the device interfaces, and also semaphore state from the GSU for when semaphore events require conversion into interrupts. The IU/IG can generate both message-signalled interrupts for host systems that can support them, and also output a dedicated interrupt request signal on pin **HIRQ_N**.

The ISU also supports conversion of interrupts to semaphore signal operations. This allows a processor core thread to synchronise to any event that causes an interrupt. The operation of the ISU is fully programmable via register control.

SRAM

The CSX600 also includes 128 Kbytes of on-chip SRAM which provides the processor with low latency access to code and data. This memory is organized as 8 K words of 16 bytes.

The memory supports fully pipelined operation, one data word per cycle, for contiguous reads or writes (to random addresses). For mixed reads and writes, the memory supports reads and writes on consecutive cycles with no dead cycles.

Typically, the SRAM is used to store items for which low-latency access from the processor core is important, such as instruction code and frequently used data. The SRAM is accessible from any bus master in the system, including the host processor.

DRAM controller & DMA

In addition to the on-chip SRAM described above, the CSX600 has an external interface for direct connection to a DDR2 DRAM array of up to 8 GBytes. This appears as another target on the system bus, and provides for bulk storage of large data sets.

The controller is fully pipelined and can maintain near-peak data bandwidths for bursts of read or write transactions, within the limitations of empty cycles caused by bank conflicts and read-write turn-around of the DRAM devices themselves.

The DRAM controller runs asynchronously to the device core, from a clock generated by a dedicated internal PLL. The multiplication ratio from the reference clock input, which it shares with the core clock PLL, is programmed by control registers.

An attached programmable DMA engine permits data transfer to or from the external DRAM to occur in the background in parallel with the processor core executing other operations. The DMA unit may be programmed by either the host processor or the device processor core. DMA transfers can be chained together via transfer description records stored anywhere in system memory. DMA operation is integrated into the hardware semaphore mechanisms for inter-processor synchronisation.

PRELIMINARY TECHNICAL DATA

Interfaces

A set of interfaces allow the CSX600 to be used in different types of systems. All interfaces are proprietary and require use of external system logic, except for the local memory interface, which connects directly to standard DDR2 DRAM devices.

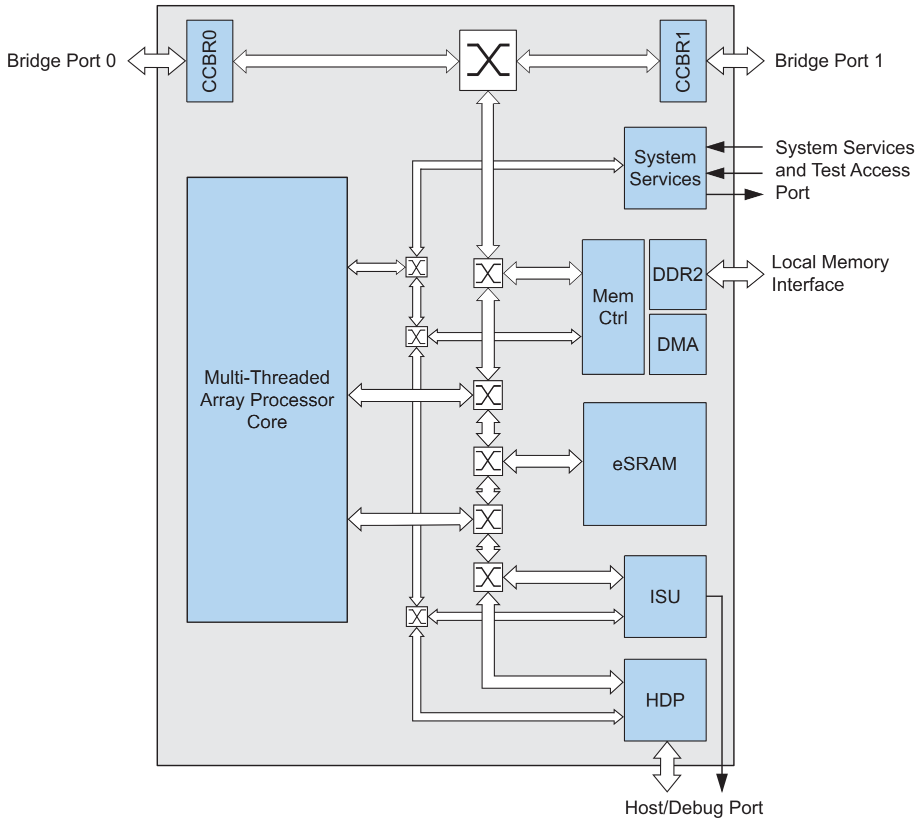

Figure 2 CSX600 external interfaces

All interfaces that carry data operate asynchronously to each other and to the processor core. This allows the clock frequency of core and all interfaces to be optimized for the application.

These interfaces are described in more detail below.

The pin counts in the headings below include analog supplies and references but not core or I/O power & ground.

CSX600 I/O signal types

The I/O pins of CSX600 have different signalling standards according to their function. All I/O pins operate from 1.8V supplies, which are separated by interface. The I/O pins all have high-side and low-side clamping diodes, and so cannot tolerate applied voltages outside of their **VDDIO** to **VSS** range. In particular, this means that I/Os are not 3.3V tolerant.

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1.8V CMOS

All configuration and control pins use 1.8V LVCMOS I/Os. Some inputs include weak pull-up resistors, those that do not must not be left floating. The LVCMOS outputs have a drive strength that self-series terminates into a 50 ohm line, and do not require parallel termination.

1.8V HSTL

The Host Debug Port is designed to operate on a multidrop bus, and all I/O pins use HSTL signalling. All signals require appropriate termination. A reference voltage is required for the HSTL input pins, and is applied to the device on its **HVREF** pin.

1.8V SSTL

The three high bandwidth ports of the device use SSTL I/O pins. The device contains programming registers that control whether the pin groups operate as SSTL class I or class II outputs. In point-to-point applications, class I is typically used. For the local memory interface, some external termination is required on address and control lines, as described below.

The SSTL pads employ on-die termination (ODT) which is controlled either by register or dynamically by the device logic, in order to eliminate the need for external termination resistors.

A reference voltage is required for all SSTL input pins. There is one **VREF** input for approximately every nine inputs.

1.8V differential SSTL clock inputs

All clock inputs on the CSX600 (except for HCLK) are differential SSTL inputs. These may be used with differential clock sources, for lowest jitter and radiated emissions. They may also be used as single ended inputs, by feeding a clock input to the CLK_P input, and tying the CLK_N input to a reference voltage in the centre of the clock signal swing, and typically VDDIO / 2.

Host interface and debug port (28 pins)

Use of the Host/Debug Port (HDP) is required for booting and controlling the device. It also provides access to the processor debug features. It has byte-wide data ports, one each for input and output. The ports are designed for multi-drop bus connections when more than one CSX600 device is used. The HDP is both a slave interface, for a host system to control the device, and a master interface, by which the device can access memory or other hardware functions that are part of host logic or associated with in-circuit debug hardware.

The HDP has its own clock input, which is typically run at a lower clock frequency than the device core. The HDP I/O pins are 1.8V class 1 HSTL, requiring external parallel termination.

The HDP uses two byte-wide interfaces for input (the *downstream* interface) and output (the *upstream* interface), and both interfaces may operate simultaneously since they share no pins, other than the clock input **HCLK**. A media access control (MAC) layer allows provision for external multidrop connection so that connecting a host or debug adaptor to multiple CSX600 chips is straightforward. The only signals wired to individual devices of a multiple processor system are pins **HREQ** and **HGNT**, all others may be connected to a common bus.

Following reset, multiple interconnected CSX600 devices are enumerated by the host system through their HDP interfaces. The host performs a special enumeration cycle to each device present by asserting **HGNT** while applying a device number to pins **HRXD[7:0]**, which identifies its unique position on the multi-device network.

Name	Width	I/O Type[a]	Description
HCLK	1	I	Clock input for HDP. All HDP I/Os are synchronous to this, except where indicated.
HREQ	1	O	Request output to arbiter. Transmitter asserts when it wishes to use upstream channel.
HGNT	1	I	Grant input from arbiter, asserted to indicate transmitter may use upstream channel.
HIRQ_N	1	OD	Interrupt request output. Asynchronous. Active low open drain.
HERR	1	OD	HDP error output, asserted for 1 or more HCLK cycles to indicate error. Active high open drain.
HRXD[7:0]	8	I	Receiver data input bus.
HRXVAL	1	I	Receiver valid data qualifier input.
HRXEOP	1	I	Receiver end of packet input.
HRXSTP	1	OD	Receiver flow control output. Active high open drain.
HVREF	1	I	Voltage reference input for all HDP pins. Nominally VDDIO2 * 0.5.
HTXD[7:0]	8	OT	Transmitter data bus output.
HTXVAL	1	IO	Transmitter data valid qualifier output. Also used as input to detect packet delineation.
HTXEOP	1	OT	Transmitter end of packet output.
HTXSTP	1	I	Transmitter flow control input.

Table 1 HDP interface signals

a. I = input, O = output, IO = input/output, OD = open drain, OT = tristate output

The HDP handles bus transactions transparently, one at a time. Each is treated as a stream of bytes, with header and data payload encoded according to the transaction type. The minimum length transaction encoding is 6 bytes. The final byte in a transaction is marked with the assertion of the corresponding EOP signal.

The HDP operates asynchronously to the device core from a dedicated clock input **HCLK**. All signals are synchronous to **HCLK** except for open drain output **HIRQ_N** which is asynchronous. The HDP contains buffering to match the slow byte-wide operation of its interfaces to the faster and wider internal bus.

All HDP I/O pads are 1.8V HSTL Class 1. Input pads require a voltage reference to applied to pin **HVREF**.

Bus bridge ports (212 pins)

Two high speed ports, Port 0 and Port 1, enable data to be transferred to and from the device. Each port is a bidirectional 90-bit wide interface that uses DDR and clock forwarding to achieve high bandwidth. The ports are a continuation of the internal ClearConnect bus, which can be 'bridged' from one device to another to form a continuous packet switching network.

Use of the bridge ports is optional. The only other data port, however, is the narrow HDP interface so most systems will use at least bridge Port 0 as a data interface to the host system or other data sources and sinks. In multi-

Name	Width	I/O Type[a]	Description
PCKIN_P	1	I	Differential clock reference input for Bridge Ports transmit clock PLL.
PCKIN_N	1	I	
P0D0CK, P0D7CK	2	IO	Bidirectional Bridge Port 0 clocks
P0D[6:1]	6	IO	Bidirectional Bridge Port 0 control
P0D[79:8]	72	IO	Bidirectional Bridge Port 0 data bus
P0S[9:0]	10	IO	Bidirectional Bridge Port 0 data strobes
P0VREF[9:0]	10	I	Port 0 voltage reference inputs
P1D0CK, P1D7CK	2	IO	Bidirectional Bridge Port 1 clocks
P1D[6:1]	6	IO	Bidirectional Bridge Port 1 control
P1D[79:8]	72	IO	Bidirectional Bridge Port 1 data bus
P1S[9:0]	10	IO	Bidirectional Bridge Port 1 data strobes
P1VREF[9:0]	10	I	Port 1 voltage reference inputs
AVDD6, AVDD4, AVDD3[b]	3	I	PLL analog supply
AVSS6, AVSS4, AVSS3	**3**	I	PLL analog ground

Table 2 Bridge port interface signals

a. I = input, IO = input/output
b. **AVDD3**,**AVDD4** and **AVSS3**,**AVSS4** used by CCBR0
AVDD6 and **AVSS6** used by CCBR1

processor systems, or where a single processor needs multiple interfaces to external logic, Port 1 may also be used. In multi-processor systems, the processors are connected in a daisy chain. If the bridge ports are not used they can be disabled to reduce power consumption.

Although the port is bidirectional, to reduce the number of pins required, upstream and downstream traffic flow independently of one another. Port direction is arbitrated by flow-control logic within the ports. When there is traffic flowing in both directions, the port will periodically reverse to share bandwidth between the flows. The ports contain buffering and programmable thresholds that can be set to optimize the bandwidth and latencies in various application modes.

The interface consists of 10 lanes of 9 signals; each lane being 8 data + 1 strobe. Data is transferred on both edges of the strobe. Signals within a lane must have their board traces closely skew matched at the higher operating speeds.

Signal lane 0 differs from the other nine groups in that it carries clocking and control information rather than data. Although the lane is the same at the physical level, the nine signals are formatted into bidirectional and unidirectional sub-groups. When configured as a down-facing port, **PnD0CK** is a forwarded clock output. The connected device will have its corresponding port configured as up-facing and there **PnD0CK** will be used as input clock reference to a deskewing PLL in the receiver data path. The forwarded clock in the reverse direction is output from the up-facing port and input to the down-facing port, this time on pin **PnD07** on both devices.

This information applies to a product under development.
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PRELIMINARY TECHNICAL DATA

Lane	Signals	Strobe
0	**PnD0CK**, **PnD7CK**, **PnD[6:1]**	**PnS[0]**
1	**PnD[15:18]**	**PnS[1]**
2	**PnD[23:16]**	**PnS[2]**
3	**PnD[31:24]**	**PnS[3]**
4	**PnD[39:32]**	**PnS[4]**
5	**PnD[47:40]**	**PnS[5]**
6	**PnD[55:48]**	**PnS[6]**
7	**PnD[63:56]**	**PnS[7]**
8	**PnD[71:64]**	**PnS[8]**
9	**PnD[79:72]**	**PnS[9]**

Table 3 Assignment of control and data signals to bus lanes

In a similar manner, signals **PnD[2:1]** are protocol signaling pins which always travel from down-facing port to up-facing port, and the corresponding signals in the opposite direction are carried on **PnD[6:5]**. Signals **PnD[4:3]** are bidirectional and reverse direction in conjunction with the data bus **PnD[79:8]**.

Pins **PnD[79:8]** in lanes 1 to 9 form a 72-bit bus which carries bus transactions in the form of header plus data payload with optional byte enables. The encoding of the header fields on to the device pins varies with transaction type.

The bridge ports transmit data paths operate asynchronously from the device core, on clocks generated by a PLL whose reference is the differential input pin pair **PCKIN_P** and **PCKIN_N**. The input clock may be applied in single-ended mode by appropriate biasing of **PCKIN_N**. In addition, the two ports may run at different, although related, clock frequencies for systems where one port is connected to an external device that must run, for example, at a lower clock speed. Clock speeds are programmed through device registers via the HDP. The receive data paths run at whatever frequency is applied as the forwarded clock from the transmit port of the device to which it is connected.

The PLLs can be bypassed by disconnecting the corresponding **AVDDn** supply.

Bridge port I/O pins

All pins are bidirectional 1.8V SSTL (JEDEC standard JESD8-15a). Typically the pins are used in Class I mode although under register control they can be operated in Class II mode. When acting as receivers the pins have on-die termination and so external termination is not required. All pads require a voltage reference input; there is one VREF pin for each of the 10 groups of signal pins.

Local memory interface (158 pins)

The CSX600 uses DDR2 DRAM for its local memory. The data interface is 64 bits wide, with an additional 8 data bits for optional error correcting code (ECC). The CSX600 DRAM controller is software configurable for a variety of DDR2 DRAM types. The clock frequency is programmable through a PLL. The device supplies the clocks and all other signals required by the DRAMs.

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Up to four ranks of devices are supported, with up to eight internal banks each, and an address width of up to fifteen bits. The interface may be operated with or without error correction, with memory width of 64 bits or 72 bits respectively. The DRAM array is operated with a DQ to DQS ratio of eight.

Name	Width	I/O Type[a]	Description
MA[14:0]	15	O	Memory address
MBA[2:0]	3	O	Memory bank address
MDQ[63:0]	64	IO	Memory data bus
MCB[7:0]	8	IO	Memory data check byte
MDM[8:0]	9	IO	Memory data masks
MDQS[8:0]	9	O	Memory data strobes
MDSG[8:0]	9	O	Memory data strobe. Should be left unconnected.
MRAS_N	1	O	Memory command
MCAS_N	1	O	
MWE_N	1	O	
MCKE	1	O	Memory clock enable
MS[3:0]_N	4	O	Memory rank selects
MODT[3:0]	4	O	Memory on-die termination control
MCK[6:0]_P	7	O	Memory differential clock outputs
MCK[6:0]_N	7	O	
MVREF[9:0]	10	I	Memory voltage reference inputs

Table 4 Local memory interface signals

a. I = input, O = output, IO = input/output

The LMI I/O pins are 1.8V SSTL operating in class I or class II, programmable via register bits for the different signal types. On-die termination is provided for all bidirectional signals.

System services (28 pins)

A collection of device resources such as clocking and reset are collectively termed System Services.

Name	Width	I/O Type[a]	Description
AVDD2-AVDD1	2	I	PLL analog supplies
AVSS2-AVSS1	2	I	PLL analog grounds
CKIN_P	1	I	Differential PLL reference input
CKIN_N	1	I	
CNFG[11:0]	12	I	Configuration bus. Sampled before and after deassertion of RST_N
RST_N	1	I	Asynchronous reset input
THDN, THDP	2	IO	Thermal monitor diode connection

Table 5 System services signals

a. I = input, IO = input/output

External pins are 1.8V LVCMOS except for **CKIN_P** and **CKIN_N** which are differential 1.8V SSTL.

Reset

The entire device is held in reset whenever the asynchronous input **RST_N** is asserted. **RST_N** should be asserted during power-up. Once **CKIN_P** (and its complement **CKIN_N**) are stable, **RST_N** may be de-asserted. Once the device has completed internal initialization with the core PLL stable, the HDP will accept access from the host system. The device may be entirely reset by asserting **RST_N** again at any time.

Clocking

The main core clock is generated by a PLL from a differential input reference clock **CKIN_P**, **CKIN_N**. The input clock may also be applied in single-ended mode by appropriate biasing of **CKIN_N**. The core clock is multiplied up by a ratio that is programmed through the configuration pins **CNFG[11:0]**. Differential inputs are provided for the PLL reference clocks to minimize jitter.

Configuration pins

Device configuration is performed via software access to control registers via the HDP interface. The device core clock, however, is configured during reset by means of 12 configuration input pins **CNFG[11:0]**. These pins are sampled both before and after de-assertion of **RST_N**, to apply 24 bits of configuration settings to the core clock PLL, such as multiplication ratio and optimization of jitter performance. See “Configuration data” on page 30 for more information.

Thermal monitor

Access to a thermal monitor diode is provided via a pair of dedicated pins, **THDN** and **THDP**. By connecting an appropriate device, such as the National Instruments LM86, this enables measurement of die temperature during operation.

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PRELIMINARY TECHNICAL DATA

Test access port (TAP)

The TAP conforms to IEEE 1149.1 and supports full EXTEST on all pins (except analog functions).

Name	Width	I/O Type[a]	Description
TCK	1	I	Test clock input
TMS	1	I	Test mode select
TDI	1	I	Test data input
TDO	1	O	Test data output
TRST_N	1	I	Test asynchronous reset. Must be pulsed or held low from power-up

Table 6 TAP signals

a. I = input, O = output

All TAP pins are 1.8V LVCMOS with weak pull-ups.

TAP instructions

There are two registers which are accessed through the TAP controller:

- Identification (read only);
- External boundary scan (IO pads).

The available TAP instructions are shown in Table 7.

Instruction Code	Instruction	Register Accessed	Description
1111	BYPASS		
0000	EXTEST	Boundary Scan	Used for test of device connectivity in assembled system
0001	SAMPLE		
0010	IDCODE	Identification	Used to identify device as part of a chain.
0100	USERCODE	User code	

Table 7 TAP instructions

Identification

The content of the (read only) CSX600 identification register is `100053EB` (hex) as defined in Table 8.

Version (4 bits)	Part Number (16 bits)	Manufacturer (11 bits)	LSB
xxxx	0000 0000 0000 0101	0011 1110 101	1

Table 8 CSX600 identification register

This information applies to a product under development. Specifications and characteristics are subject to change without notice.

All CSX600 parts will have the same **Part Number** field; the **Version** field will be updated for each revision.

The content of the (read only) CSX600 user code register value is 0000500B (hex).

DC and thermal characteristics

Recommended operating conditions

Parameter		Test Conditions	Min	Typ	Max	Units
VDD	Core supply voltage		1.14	1.2	1.26	V
VDDIO	External (I/O) supply voltages		1.65	1.8	1.95	V
AVDD	Analog supply voltages			1.5		V
Tcase	Case temperature		0		70	°C
Tdie	Die temperature		0		100	°C

Table 9 Recommended operating conditions

Supply sequencing

The voltage applied to **VDD** must never exceed the voltage applied to any of the **VDDIO** supplies. Particular care should be taken to ensure that **VDD** is never driven higher than **VDDIO** during power-up and power-down.

To avoid the possibility of damage to I/O pads, no I/O signal should have voltages applied outside of their corresponding **VDDIO** supply. Particular care should be taken at power-up not to apply signals to I/O pins before **VDDIO** is applied. The applied I/O voltage may track the rise of **VDDIO**, as long as the Absolute Maximum ratings are observed.

Handling and assembly

The CSX600 meets JEDEC MSL (Moisture Sensitivity Level) 4. Once removed from the moisture-proof packaging, the components have a floor life of 72 hours (at or below 30°C / 60% relative humidity). After this they will require rebaking at 125°C for 24 hours.

Warning: ESD (electrostatic discharge) sensitive device

Electrostatic charges of up to several thousand volts can accumulate on test equipment and the human body, and can discharge without detection. Although the CSX600 includes ESD protection circuitry, permanent damage may be caused to devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid damage and loss of functionality.

Absolute maximum ratings

Core supply voltage (**VDD**) . . . . -0.3V to +1.6V

External I/O supply voltages (**VDDIO**) . . . . -0.3V to +1.95V

Analog supply voltages (**AVDD**) . . . . -0.3V to +1.6V

Minimum input voltage **VSS**-0.3V

Maximum input voltage . . . . **VDDIO**+0.3V

Operating die temperature . . . . 125°C

This information applies to a product under development.
Specifications and characteristics are subject to change without notice.

Soldering temperature[1] . . . . 250°C

Storage temperature . . . . -65°C to +150°C

Note: These are stress ratings only. Conditions beyond those listed above may cause permanent damage to the device. Functional operation at these or any other conditions outside the normal operating range is not implied. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Termination & reference voltages

HDP

HDP I/O pads are 1.8V HSTL signals. And the pads require a voltage reference of 1/2 VDD IO. The **VREF** signal must be decoupled at the pin, and the signal kept away from sources of interference.

CCBR

CCBR pins are 1.8V bidirectional SSTL signals. When acting as receivers the pins have on-die termination and so in most applications external termination is not required. Because of this all pads require a voltage reference input of 1/2 **VDDIO**; there is one **VREF** pin for each of the 10 groups of signal pins. **VREF** signals must be decoupled at the pin, and the signal kept away from sources of interference.

The **PCKIN_P** and **PCKIN_N** pins both have internal split termination of 150 ohm to **VDDIO2** and 150 ohm to **VSS**.

LMI

LMI pins are 1.8V bidirectional SSTL signals. When acting as receivers the pins have on-die termination and so in most applications external termination is not required. The memory reference voltage, **MVREF**, requires a voltage level of 1/2 **VDDIO**. **VREF** signals must be decoupled at the pin, and the signal kept away from sources of interference.

Analog supplies

The PLLs on the chip require a low noise 1.5V supply to avoid clock jitter. The requirements for analog supply decoupling are shown in Figure 3. An LC pair as shown is required for every **AVDDn** pin that is powered. Example component types for L and C are shown in Table 10. These must be located right next to each power pin.

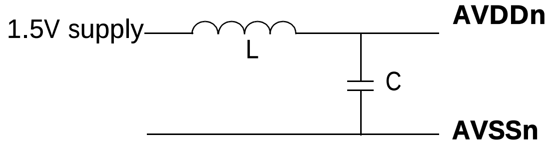

Figure 3 Analog supply decoupling

1. For lead-free e1 parts using SnAgCu BGA balls

This information applies to a product under development.
Specifications and characteristics are subject to change without notice.

Component	Example
L	Murata BLM15AG601SN1D
C	Murata GRM155R60J105KE19

Table 10 Example decoupling components

LVCMOS DC characteristics

Parameter		Test Conditions	Min	Typ	Max	Units
VIH	High Level Input Voltage		0.65 * VDDIO		1.95	V
VIL	Low Level Input Voltage		0		0.35 * VDDIO	V

Table 11 DC characteristics for LVCMOS pins

HSTL DC characteristics

Parameter		Test Conditions	Min	Typ	Max	Units
VIH	High Level Input Voltage		0.65 * VDDIO		1.95	V
VIL	Low Level Input Voltage		0		0.35 * VDDIO	V

Table 12 DC characteristics for HSTL pins

SSTL DC characteristics

Parameter		Test Conditions	Min	Typ	Max	Units
VIN	DC Input Signal Voltage		-0.3		VDDIO + 0.3	V
VID	DC Differential Input Voltage		0.25		VDDIO + 0.6	V

Table 13 DC characteristics for SSTL pins

Reference voltages

TBD

PRELIMINARY TECHNICAL DATA

AC characteristics

Test conditions

All output timings are measured driving a 50 ohm resistive load.

System services

Name	Min	Max	Comment	Units
tCK	10	30	Period, core reference clock **CKIN_P, CKIN_N**	ns
tCKH	3		Pulse width high, core reference clock **CKIN_P, CKIN_N**	ns
tCKL	3		Pulse width low, core reference clock **CKIN_P, CKIN_N**	ns
		100	Cycle-cycle jitter, core reference clock **CKIN_P, CKIN_N**	ps
tRST	100		**RST_N** assertion pulse width	ns
tCKR	0		CKIN stable to **RST_N** deassertion	ns
tCSU	10		Setup, **CNFG** to **RST_N** deassertion	ns
tCH	10		Hold, **RST_N** deassertion to **CNFG**	ns

Table 14 System services timing parameters

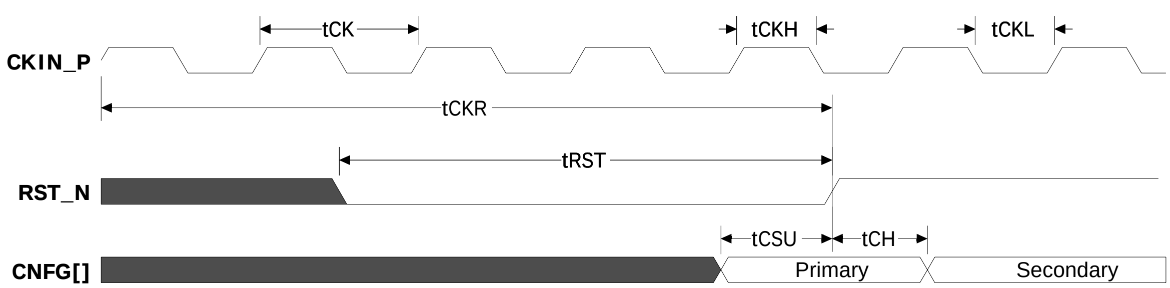

Figure 4 Reset and configuration timing

This information applies to a product under development. Specifications and characteristics are subject to change without notice.

PRELIMINARY TECHNICAL DATA

Host interface and debug port

All HDP timings are relative to synchronous input clock **HCLK**.

Name	Min	Max	Comment	Units
tHCK	6.0		Period, clock input **HCLK**	ns
tHSU	1.0		Setup, input to **HCLK**	ns
tHH	0.9		Hold, input from **HCLK**	ns
tHCO	0.5	3.0	Delay, **HCLK** to any output	ns

Table 15 HDP timing parameters

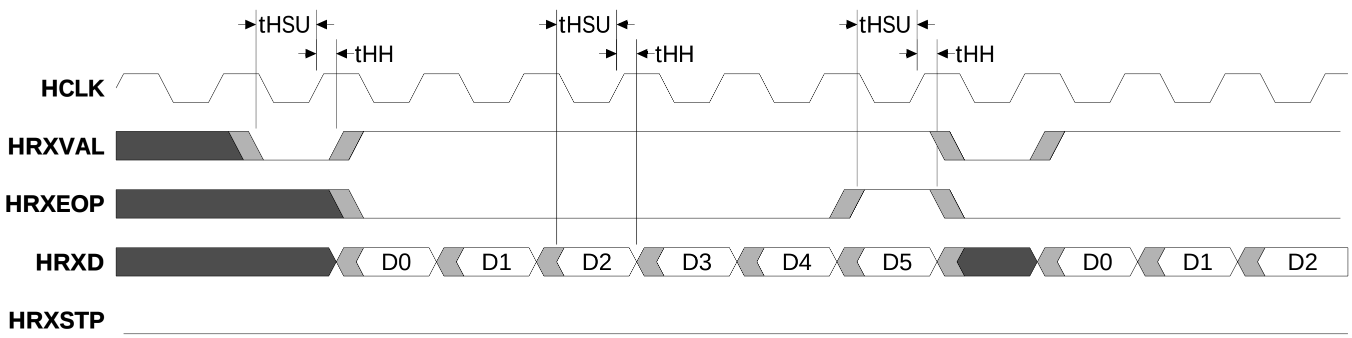

Figure 5 Host/debug port packet receive

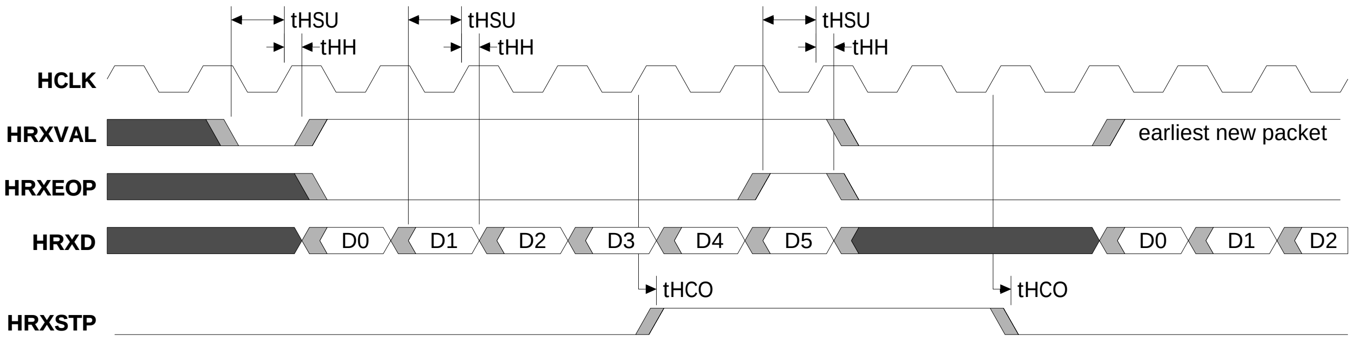

Figure 6 Host/debug port packet receive with flow control

This information applies to a product under development.
Specifications and characteristics are subject to change without notice.

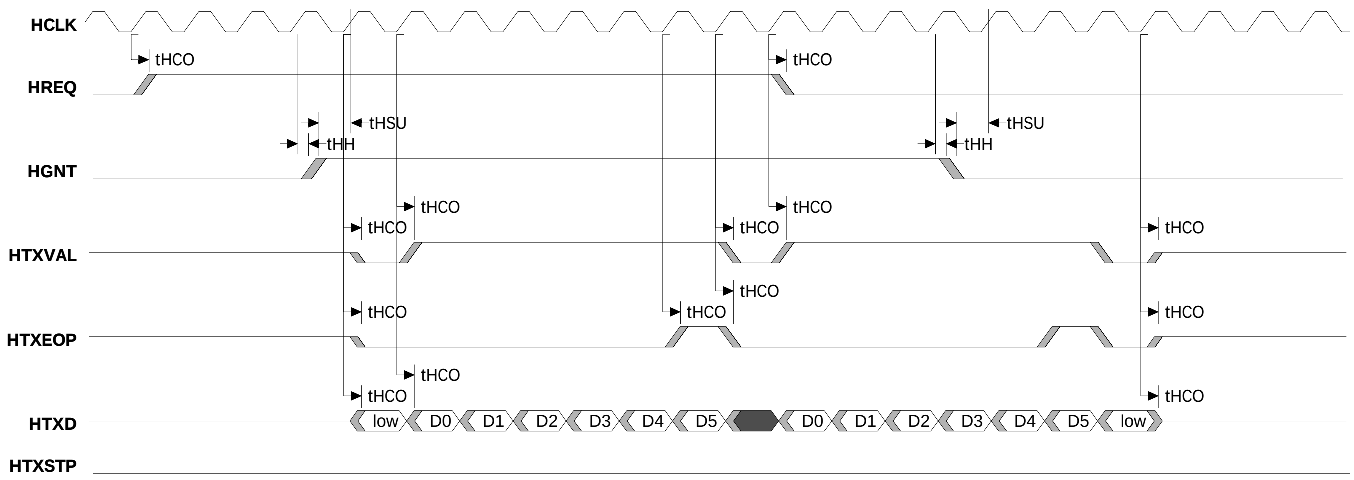

Figure 7 Host/debug port packet transmit

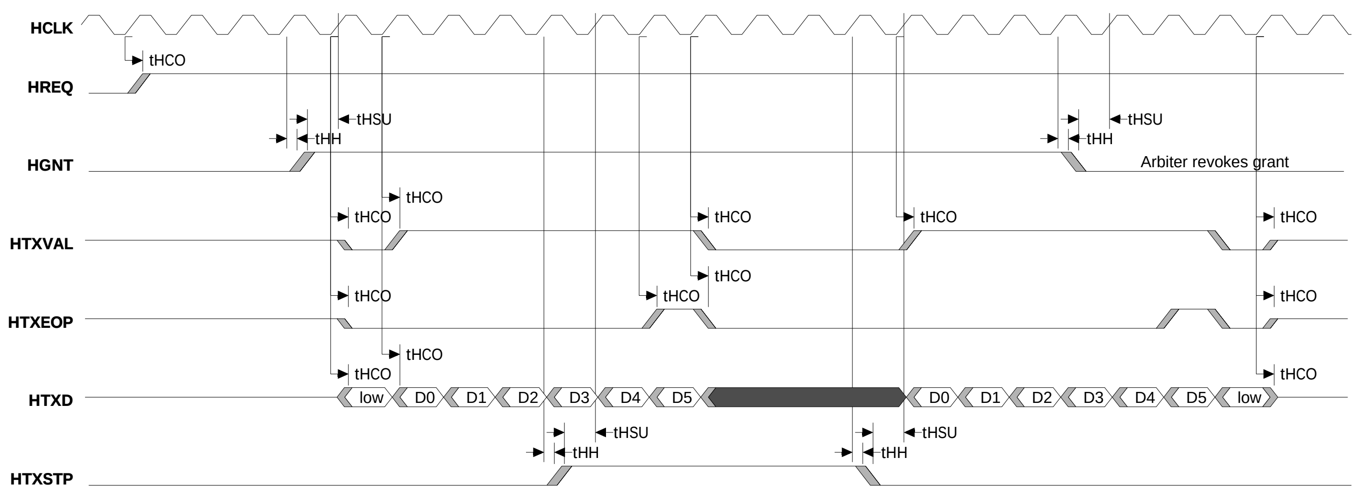

Figure 8 Host/debug port packet transmit with flow control and grant revocation

This information applies to a product under development. Specifications and characteristics are subject to change without notice.

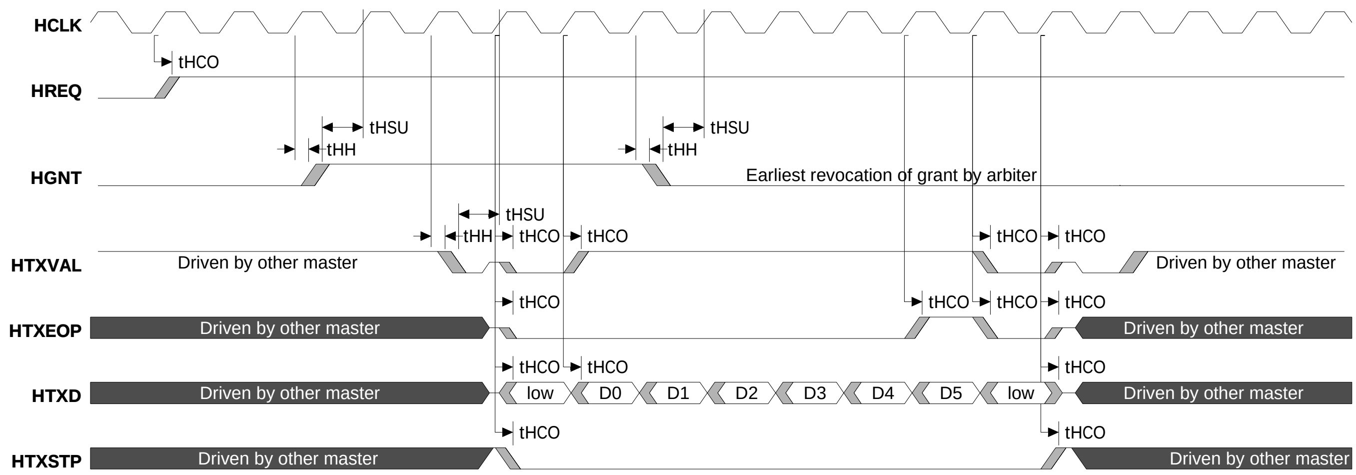

Figure 9 Host/debug port transmit arbitration

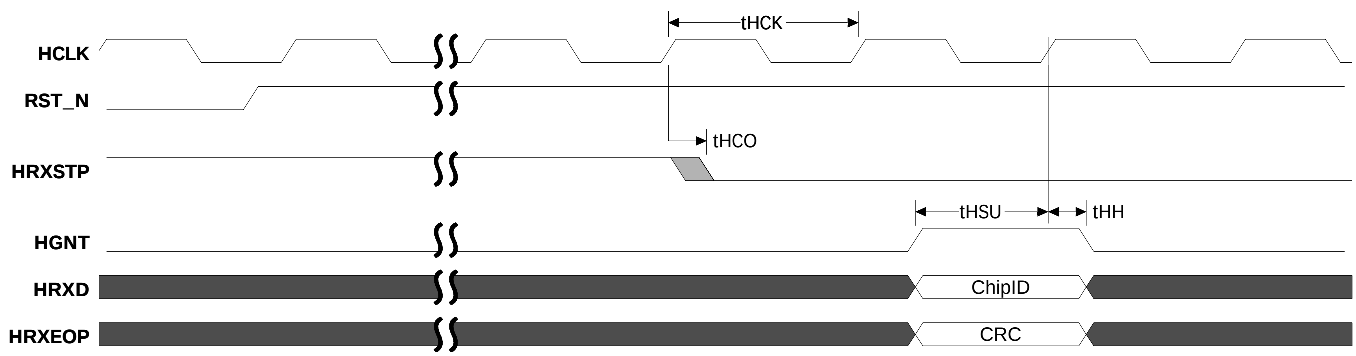

Figure 10 Host/debug port initialization

Bridge ports

The two bridge ports have identical but fully independent timing parameters. They may be programmed to operate at the same or different transmit clock frequencies. In the tables below, signal names refer to Port 0 only. Port 1 timing is identical.

Name	Min	Max	Comment	Units
tPCK	10	30	Period, bridge port transmit reference clock **PCKIN_P, PCKIN_N**	ns
tPCKH	3		Pulse width high, bridge port transmit reference clock **PCKIN_P, PCKIN_N**	ns
tPCKL	3		Pulse width low, bridge port transmit reference clock **PCKIN_P, PCKIN_N**	ns
		100	Cycle-cycle jitter, bridge port transmit reference clock **PCKIN_P, PCKIN_N**	ps
tPP	2.5		Transmit data bit period.[a]	ns
tPCSO		+/-0.25	Output skew, transmit clock to any transmit strobe.	ns
tPDSO	0.8		Delay, transmit data out to strobe out rising/falling, same lane.[b]	ns
tPSDO			Delay, strobe out rising/falling to transmit data out, same lane.	ns
tPZDO		2*tPP+0.5	Data driven to first data valid, any lane.	ns
tPDZO		2*tPP+0.5	Final data valid to data tristate.	ns
tPCKI	5.0		Period, receive clock in.	ns
tPCSI		+/-1.25	Input skew, receive clock to any receive strobe.	ns
tPSU	0.3		Setup, input data valid to input strobe rising/falling, same lane.	ns
tPH	0.3		Hold, input strobe rising/falling to input data invalid, same lane.	ns

Table 16 Bridge Port timing parameters

a. tPP is defined by the programming of the Bridge Port clock generator PLL, and the input clock frequency on **PCKIN**.
b. At minimum tPP.

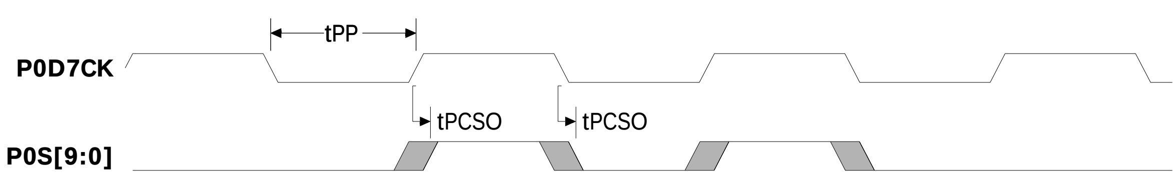

Figure 11 Bridge port transmit clock and transmit strobes

Note: Transmit clock is **P0D7CK** or **P0D0CK** with port configured for up-facing or down-facing operation respectively.

This information applies to a product under development. Specifications and characteristics are subject to change without notice.

PRELIMINARY TECHNICAL DATA

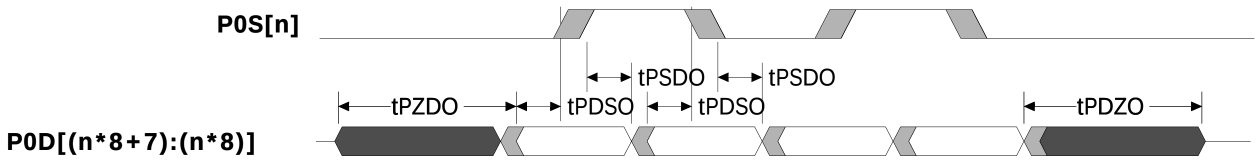

Figure 12 Bridge port transmit data & strobe (same lane)

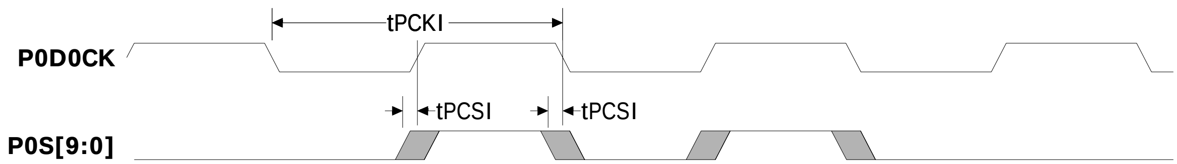

Figure 13 Bridge port receive clock and receive strobes

Note: Receive clock is **P0D0CK** or **P0D7CK** with port configured for up-facing or down-facing operation respectively.

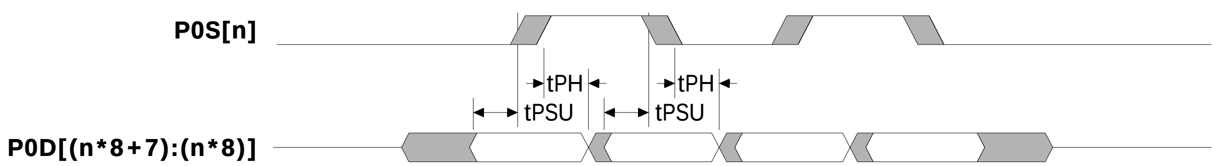

Figure 14 Bridge port receive data & strobe (same lane)

This information applies to a product under development.
Specifications and characteristics are subject to change without notice.

Local memory interface

Name	Min	Typ	Max	Comment	Units
tMCK		5		Clock output period	ns
tMCSO	-1.25		1.25	Output skew any transmit clock to any data strobe	ns
tMCRR	RL[a]	RL+4.5		Clock out to strobe in	ns
tMDSO	-0.75		0.75	Transmit data to stobe out rising/falling same lane	ns
tMSU	0.4				ns
tMH	0.4				ns
tMDSS					ns
tMWPRE	1.5			Data strobe preamble	ns
tMWPST	2			Data strobe post-amble	ns
tMCAOSU	0.8			Delay from control/address edge to following clock rising edge	ns
tMCAOH	1			Delay from clock rising edge to control/address edge	ns

Table 17 Local memory interface timing parameters

a. RL = read latency

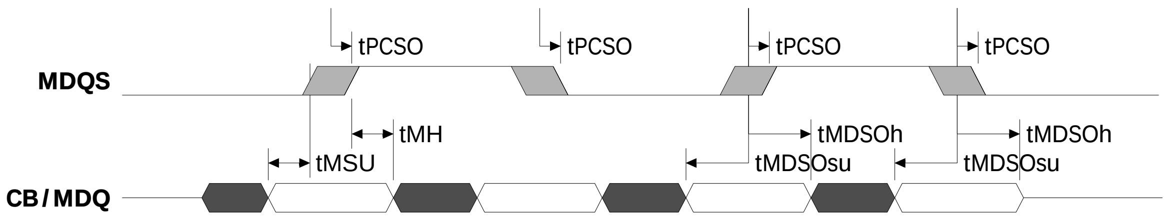

Figure 15 Local memory interface rx

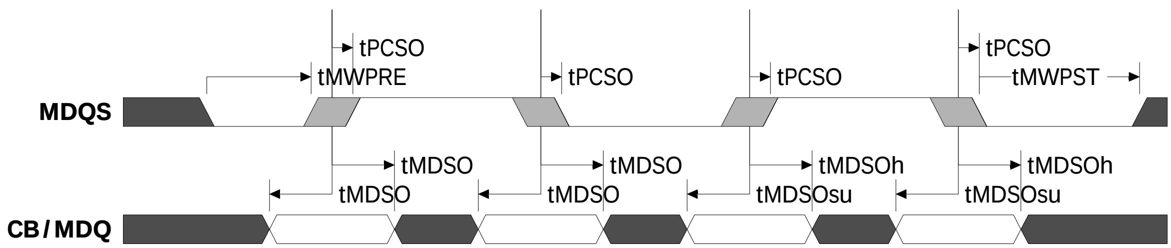

Figure 16 Local memory interface tx

This information applies to a product under development. Specifications and characteristics are subject to change without notice.

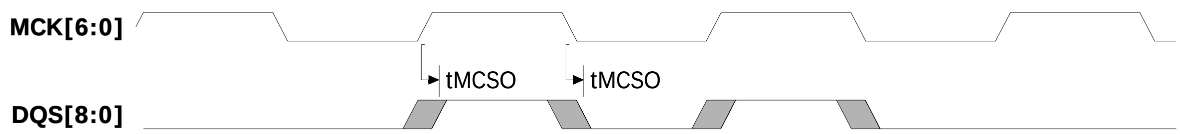

Figure 17 Local memory interface tx clk

Test access port

The operation of the IEEE1149.1 TAP is independent of the other device interfaces.

Name	Min	Max	Comment	Units
tTRST	100		**TRST_N** assertion pulse width	ns
tTSDC	5		**TMS**, **TDI** setup before **TCK** rising	ns
tTHCD	0		**TMS**, **TDI** hold after **TCK** rising	ns
tTCCYC	100		**TCK** period rising to rising	ns
tTCPW	20		**TCK** high pulse width	ns
tTCO	1	10	**TCK** falling to **TDO** valid delay	ns

Table 18 Test access port timing parameters

.

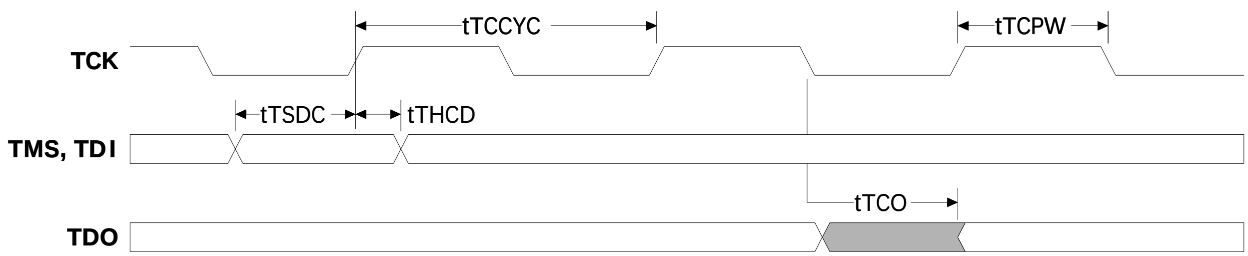

Figure 18 Test access port timing

Bootstrap sequence

The usual initialization and bootstrap sequence is summarized below.

1. Apply power. The supplies should be applied in the following sequence: **VDDIO** → **AVDD** → **VDD**.
2. Assert **RST_N**. This puts the following subsystems into the reset state:
    - All PLLs
    - All control registers
    - Local memory interface
    - Bridge Port logic
    - Bridge Port I/Os
    - Host / Debug Port
    - System services
    - Core logic

   RST_N must remain asserted until **CKIN_P, CKIN_N** have a stable clock.
3. Set the PLL configuration signals **CNFG[11:0]** to the required state for the primary configuration data.
4. De-assert **RST_N**.
5. Set the PLL configuration signals **CNFG[11:0]** to the required state for the secondary configuration data.
6. The core clock PLL takes a number of **CLKIN** cycles to stabilize the core clock. The following subsystems are still in the reset state at this point:
    - LMI and Bridge Port PLLs
    - Local memory interface
    - Bridge Port logic
    - Bridge Port I/O
    - Host / Debug Port
7. When core clock has stabilized, the output signal **HRXSTP** is de-asserted, indicating to the host logic that the HDP port is ready to accept the bus enumeration and subsequent access to internal device registers.
8. Enumerate the device ID via the HDP, by applying ID to **HRXD[7:0]** and asserting **HGNT** for one cycle.
9. Configure the Bridge Ports control registers via the HDP.
    a. Configure Bridge Ports
    b. Configure transmit PLL.
    c. Wait for at least 100us
    d. Take Bridge Port I/O out of reset by writing to **CCBRIOCTRL** register
    e. Configure receive PLL
    f. Wait for at least 100us
    g. Take transmit Bridge Port logic out of reset by writing to **CCBRCTRL** register
    h. Take receive Bridge Port logic out of reset by writing to **CCBRCTRL** register
10. Configure the LMI.
11. Configure the Address Expansion Units in the ClearConnect bus.
12. Configure the Interrupt and Semaphore Unit.
13. Boot processor core.

This information applies to a product under development.
Specifications and characteristics are subject to change without notice.

Configuration data

Unlike all other device operating modes, which are programmable through internal registers, the PLL that generates the core clock must be configured directly from external pins since it is itself required for access to the configuration registers. Configuration pins **CNFG[11:0]** are used for this purpose. 24 bits of configuration data are applied in two sets: the twelve *primary* bits are sampled by the device on the de-assertion of reset. These define the multiplication ratio of the reference clock to the internal core clock. The ratio does not have to be an integer; low order fractional ratios are also possible. The twelve *secondary* bits must then be applied continuously from a short period after reset. These bits adjust the analog parameters of the PLL, and are set for lowest jitter. Table 19 shows the different fields that make up the configuration patterns.

<table>
<tr><th>CNFG bits</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>Primary</td><td>0</td><td>FB-SEL</td><td colspan="3">RANGEB</td><td colspan="3">RANGEA</td><td colspan="4">MULT</td></tr>
<tr><td>Secondary</td><td>0</td><td>0</td><td>0</td><td colspan="9">TUNE</td></tr>
</table>

Table 19 PLL configuration fields

The meaning of these bit fields is as follows:

MULT: feedback divider

RANGEA: output A divider

RANGEB: output B divider

FBSEL: select output A or B for feedback

TUNE: VCO filter setting

For the normal operating case of a 50 MHz input clock and 250 MHz core clock, the required values are:

Primary: 000110110101

Secondary: 000111011100

This information applies to a product under development.
Specifications and characteristics are subject to change without notice.

PRELIMINARY TECHNICAL DATA

Mechanical data

The CSX600 is available in a 1,011 pin thermally-enhanced Ball Grid Array (BGA) package. Mechanical details are shown in Figure 19.

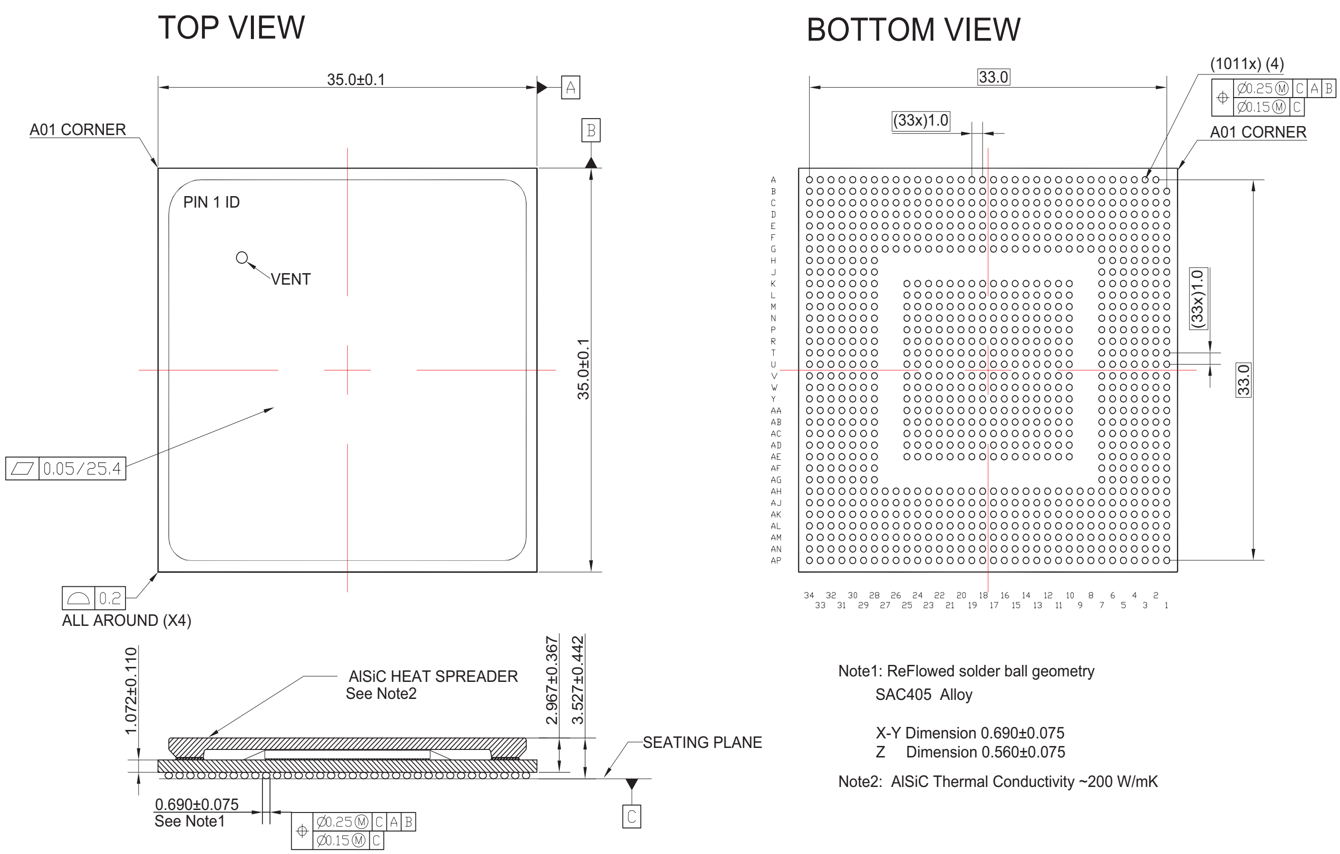

Figure 19 Mechanical data

This information applies to a product under development.
Specifications and characteristics are subject to change without notice.

Pin assignment

Table 20 summarizes the function assigned to every pin of the device. Tables 21 to 27 show the pinout organized by function.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A3	**MDQ12**	A4	**MDQ8**	A5	**MCK4_N**	A6	**MCK1_N**	A7	**MDQ14**	A8	**MDQ21**	A9	**MDQ17**
A10	**MDQS2**	A11	**MDQ28**	A12	**MDQ24**	A13	**MDSG3**	A14	**MDQ30**	A15	**MCK3_N**	A16	**MCK0_N**
A17	**NC**	A18	**MCB0**	A19	**MDQS8**	A20	**MCB7**	A21	**MCB3**	A22	**MDQ37**	A23	**MDM4**
A24	**MDSG4**	A25	**MDQ39**	A26	**MDQ35**	A27	**MDQ41**	A28	**MDQ46**	A29	**MDQ43**	A30	**MCK2_P**
A31	**MCK5_P**	A32	**MDSG6**	A33	**MDM6**	B3	**MDQ3**	B5	**MCK4_P**	B6	**MCK1_P**	B8	**MDQ20**
B9	**MDSG2**	B11	**MDQ29**	B12	**MDQ25**	B14	**MDM3**	B15	**MCK3_P**	B16	**MCK0_P**	B17	**NC**
B19	**MCB6**	B21	**MCB2**	B22	**MDQ32**	B24	**MDQS4**	B25	**MDQ34**	B27	**MDSG5**	B28	**MDQ47**
B30	**MCK2_N**	B31	**MCK5_N**	B33	**MDQS6**	C1	**MDQ7**	C2	**MDQ2**	C4	**MDQ13**	C5	**MDSG1**
C7	**MDQS1**	C8	**MDQ10**	C10	**MDM2**	C11	**MDQ23**	C13	**MDQS3**	C14	**MDQ31**	C16	**MDQ27**
C17	**MA1**	C18	**MCB1**	C19	**MDSG8**	C21	**MDQ36**	C22	**MDQ33**	C24	**MDQ38**	C25	**MDQ45**
C27	**MDM5**	C28	**MDQ42**	C30	**MDQ53**	C31	**MDQ49**	C32	**MDQ50**	C33	**MDQ55**	C34	**MDQ54**
D1	**MDQS0**	D3	**MDQ6**	D5	**MDQ9**	D6	**MDM1**	D8	**MDQ15**	D9	**MDQ16**	D11	**MDQ22**
D12	**MDQ18**	D14	**MA8**	D15	**MDQ19**	D17	**MA2**	D18	**MA0**	D20	**MA10**	D21	**MRAS_N**
D23	**MCAS_N**	D24	**MDQ44**	D26	**MDQ40**	D27	**MDQS5**	D29	**MDQ52**	D30	**MDQ48**	D32	**MDQ51**
D34	**MDQ61**	E1	**MDQ1**	E2	**MDSG0**	E4	**MDQ0**	E7	**NC**	E8	**MBA2**	E10	**MDQ11**
E11	**MA9**	E13	**MA7**	E14	**MA6**	E16	**MA5**	E18	**MCB5**	E19	**MDM8**	E21	**MODT0**
E22	**MWE_N**	E24	**MS2_N**	E25	**MODT1**	E27	**MODT2**	E28	**MODT3**	E30	**MDQ60**	E31	**MDQ56**
E33	**MDQ57**	E34	**MDSG7**	F1	**MDQ5**	F3	**MDM0**	F5	**MDQ4**	F6	**MCKE**	F8	**MA14**
F11	**MA12**	F12	**MA11**	F15	**MDQ26**	F16	**MA4**	F17	**MA3**	F18	**MCB4**	F19	**MS0_N**
F20	**MBA1**	F21	**MBA0**	F23	**MS1_N**	F24	**MA13**	F26	**MS3_N**	F28	**MDQ58**	F29	**MDQ63**
F30	**MDQS7**	F32	**MDQ62**	F33	**MDM7**	F34	**MCK6_P**	G1	**RST_N**	G3	**NC**	G4	**CNFG0**
G10	**MVREF0**	G11	**MVREF1**	G13	**MVREF2**	G14	**MVREF3**	G16	**MVREF9**	G17	**MVREF8**	G21	**MVREF4**
G22	**MVREF5**	G24	**MVREF6**	G25	**MVREF7**	G32	**MDQ59**	G34	**MCK6_N**	H2	**NC**	H4	**CNFG1**
H5	**CNFG7**	H7	**NC**	H29	**HTXEOP**	H30	**HTXSTP**	H31	**HTXD6**	H33	**HTXD1**	H34	**HTXD0**
J1	**CKIN_P**	J3	**NC**	J4	**CNFG2**	J5	**CNFG8**	J6	**NC**	J7	**NC**	J28	**HCLK**
J30	**HGNT**	J32	**HTXD5**	J34	**HTXD2**	K1	**CKIN_N**	K3	**NC**	K4	**CNFG3**	K5	**CNFG9**
K7	**THDP**	K18	**NC**	K29	**HTXVAL**	K30	**HREQ**	K31	**HTXD7**	K33	**HTXD4**	K34	**HTXD3**
L4	**CNFG4**	L5	**CNFG10**	L6	**NC**	L7	**THDN**	L18	**NC**	L29	**HRXEOP**	L30	**HRXSTP**
L31	**HRXD6**	L33	**HRXD1**	L34	**HRXD0**	M1	**TCK**	M2	**TDI**	M3	**TRST_N**	M4	**CNFG5**
M5	**CNFG11**	M28	**HVREF**	M30	**HERR**	M31	**HRXVAL**	M32	**HRXD5**	M33	**HRXD3**	M34	**HRXD2**
N1	**TMS**	N2	**TDO**	N4	**CNFG6**	N5	**PUP**	N6	**NC**	N7	**NC**	N29	**HIRQ_N**
N31	**HRXD7**	N33	**HRXD4**	P1	**P0D8**	P3	**P0D9**	P5	**P0D10**	P7	**VSS**	P28	**P1VREF1**
P30	**P1D10**	P32	**P1D9**	P34	**P1D8**	R2	**P0D11**	R4	**P0S1**	R6	**P0D12**	R10	**AVDD1**
R11	**AVSS1**	R29	**P1D12**	R31	**P1S1**	R33	**P1D11**	T1	**P0D13**	T3	**P0D14**	T5	**P0D15**
T7	**P0VREF1**	T10	**AVDD2**	T11	**AVSS2**	T30	**P1D15**	T32	**P1D14**	T34	**P1D13**	U2	**P0D16**
U4	**P0D17**	U6	**P0D18**	U29	**P1D18**	U31	**P1D17**	U33	**P1D16**	V1	**P0D19**	V3	**P0S2**
V5	**P0D20**	V28	**P1VREF2**	V30	**P1D20**	V32	**P1S2**	V34	**P1D19**	W2	**P0D21**	W4	**P0D22**
W6	**P0D23**	W7	**P0VREF2**	W29	**P1D23**	W31	**P1D22**	W33	**P1D21**	Y1	**P0D24**	Y3	**P0D25**
Y5	**P0D26**	Y28	**P1VREF3**	Y30	**P1D26**	Y32	**P1D25**	Y34	**P1D24**	AA2	**P0D27**	AA4	**P0S3**
AA6	**P0D28**	AA29	**P1D28**	AA31	**P1S3**	AA33	**P1D27**	AB1	**P0D29**	AB3	**P0D30**	AB5	**P0D31**
AB7	**P0VREF3**	AB30	**P1D31**	AB32	**P1D30**	AB34	**P1D29**	AC2	**P0D32**	AC4	**P0D33**	AC6	**P0D34**
AC29	**P1D34**	AC31	**P1D33**	AC33	**P1D32**	AD1	**P0D35**	AD3	**P0S4**	AD5	**P0D36**	AD13	**AVSS3**

Table 20 Pin assignment

This information applies to a product under development.
Specifications and characteristics are subject to change without notice.

PRELIMINARY TECHNICAL DATA

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
AD17	**AVSS4**	AD18	**VSS**	AD22	**AVSS6**	AD28	**P1VREF4**	AD30	**P1D36**	AD32	**P1S4**	AD34	**P1D35**
AE2	**P0D37**	AE4	**P0D38**	AE6	**P0D39**	AE7	**P0VREF4**	AE13	**AVDD3**	AE17	**AVDD4**	AE18	**VSS**
AE22	**AVDD6**	AE29	**P1D39**	AE31	**P1D38**	AE33	**P1D37**	AF1	**P0D40**	AF3	**P0D41**	AF5	**P0D42**
AF28	**P1VREF5**	AF30	**P1D42**	AF32	**P1D41**	AF34	**P1D40**	AG2	**P0D43**	AG4	**P0S5**	AG6	**P0D44**
AG7	**P0VREF5**	AG29	**P1D44**	AG31	**P1S5**	AG33	**P1D43**	AH1	**P0D45**	AH3	**P0D46**	AH5	**P0D47**
AH9	**P0VREF7**	AH11	**P0VREF6**	AH12	**P0VREF0**	AH14	**P0VREF8**	AH15	**P0VREF9**	AH20	**P1VREF9**	AH21	**P1VREF8**
AH23	**P1VREF0**	AH24	**P1VREF6**	AH26	**P1VREF7**	AH30	**P1D47**	AH32	**P1D46**	AH34	**P1D45**	AJ2	**P0D58**
AJ4	**P0D63**	AJ6	**P0D52**	AJ8	**P0D2**	AJ10	**P0D7CK**	AJ12	**P0D68**	AJ14	**P0D74**	AJ16	**P0D79**
AJ19	**P1D79**	AJ21	**P1D74**	AJ23	**P1D68**	AJ25	**P1D7CK**	AJ27	**P1D2**	AJ29	**P1D52**	AJ31	**P1D63**
AJ33	**P1D58**	AK3	**P0D60**	AK5	**P0D50**	AK7	**P0D55**	AK9	**P0D4**	AK11	**P0D66**	AK13	**P0D71**
AK15	**P0D76**	AK20	**P1D76**	AK22	**P1D71**	AK24	**P1D66**	AK26	**P1D4**	AK28	**P1D55**	AK30	**P1D50**
AK32	**P1D60**	AL2	**P0D57**	AL4	**P0D62**	AL6	**P0S6**	AL8	**P0D1**	AL10	**P0D6**	AL12	**P0S8**
AL14	**P0D73**	AL16	**P0D78**	AL19	**P1D78**	AL21	**P1D73**	AL23	**P1S8**	AL25	**P1D6**	AL27	**P1D1**
AL29	**P1S6**	AL31	**P1D62**	AL33	**P1D57**	AM3	**P0S7**	AM5	**P0D49**	AM7	**P0D54**	AM9	**P0S0**
AM11	**P0D65**	AM13	**P0D70**	AM15	**P0S9**	AM17	**NC**	AM18	**NC**	AM20	**P1S9**	AM22	**P1D70**
AM24	**P1D65**	AM26	**P1S0**	AM28	**P1D54**	AM30	**P1D49**	AM32	**P1S7**	AN2	**P0D56**	AN4	**P0D61**
AN6	**P0D51**	AN8	**P0D0CK**	AN10	**P0D5**	AN12	**P0D67**	AN14	**P0D72**	AN16	**P0D77**	AN19	**P1D77**
AN21	**P1D72**	AN23	**P1D67**	AN25	**P1D5**	AN27	**P1D0CK**	AN29	**P1D51**	AN31	**P1D61**	AN33	**P1D56**
AP3	**P0D59**	AP5	**P0D48**	AP7	**P0D53**	AP9	**P0D3**	AP11	**P0D64**	AP13	**P0D69**	AP15	**P0D75**
AP17	**PCKIN_P**	AP18	**PCKIN_N**	AP20	**P1D75**	AP22	**P1D69**	AP24	**P1D64**	AP26	**P1D3**	AP28	**P1D53**
AP30	**P1D48**	AP32	**P1D59**										

Table 20 Pin assignment

Signal	Pin	Dir	Type	Signal	Pin	Dir	Type
PCKIN_N	AP18	I	SSTL	**PCKIN_P**	AP17	I	SSTL

Table 21 Common bridge port signals

Signal	Pin	Dir	Type	Signal	Pin	Dir	Type	Signal	Pin	Dir	Type
AVDD3	AE13	I	ANALOG	**AVDD4**	AE17	I	ANALOG	**AVSS3**	AD13	I	ANALOG
AVSS4	AD17	I	ANALOG	**P0D0CK**	AN8	IO	SSTL	**P0D1**	AL8	IO	SSTL
P0D10	P5	IO	SSTL	**P0D11**	R2	IO	SSTL	**P0D12**	R6	IO	SSTL
P0D13	T1	IO	SSTL	**P0D14**	T3	IO	SSTL	**P0D15**	T5	IO	SSTL
P0D16	U2	IO	SSTL	**P0D17**	U4	IO	SSTL	**P0D18**	U6	IO	SSTL
P0D19	V1	IO	SSTL	**P0D2**	AJ8	IO	SSTL	**P0D20**	V5	IO	SSTL
P0D21	W2	IO	SSTL	**P0D22**	W4	IO	SSTL	**P0D23**	W6	IO	SSTL
P0D24	Y1	IO	SSTL	**P0D25**	Y3	IO	SSTL	**P0D26**	Y5	IO	SSTL
P0D27	AA2	IO	SSTL	**P0D28**	AA6	IO	SSTL	**P0D29**	AB1	IO	SSTL
P0D3	AP9	IO	SSTL	**P0D30**	AB3	IO	SSTL	**P0D31**	AB5	IO	SSTL
P0D32	AC2	IO	SSTL	**P0D33**	AC4	IO	SSTL	**P0D34**	AC6	IO	SSTL
P0D35	AD1	IO	SSTL	**P0D36**	AD5	IO	SSTL	**P0D37**	AE2	IO	SSTL
P0D38	AE4	IO	SSTL	**P0D39**	AE6	IO	SSTL	**P0D4**	AK9	IO	SSTL
P0D40	AF1	IO	SSTL	**P0D41**	AF3	IO	SSTL	**P0D42**	AF5	IO	SSTL
P0D43	AG2	IO	SSTL	**P0D44**	AG6	IO	SSTL	**P0D45**	AH1	IO	SSTL
P0D46	AH3	IO	SSTL	**P0D47**	AH5	IO	SSTL	**P0D48**	AP5	IO	SSTL
P0D49	AM5	IO	SSTL	**P0D5**	AN10	IO	SSTL	**P0D50**	AK5	IO	SSTL

Table 22 Bridge port 0 signals

This information applies to a product under development.
Specifications and characteristics are subject to change without notice.

PRELIMINARY TECHNICAL DATA

Signal	Pin	Dir	Type	Signal	Pin	Dir	Type	Signal	Pin	Dir	Type
P0D51	AN6	IO	SSTL	**P0D52**	AJ6	IO	SSTL	**P0D53**	AP7	IO	SSTL
P0D54	AM7	IO	SSTL	**P0D55**	AK7	IO	SSTL	**P0D56**	AN2	IO	SSTL
P0D57	AL2	IO	SSTL	**P0D58**	AJ2	IO	SSTL	**P0D59**	AP3	IO	SSTL
P0D6	AL10	IO	SSTL	**P0D60**	AK3	IO	SSTL	**P0D61**	AN4	IO	SSTL
P0D62	AL4	IO	SSTL	**P0D63**	AJ4	IO	SSTL	**P0D64**	AP11	IO	SSTL
P0D65	AM11	IO	SSTL	**P0D66**	AK11	IO	SSTL	**P0D67**	AN12	IO	SSTL
P0D68	AJ12	IO	SSTL	**P0D69**	AP13	IO	SSTL	**P0D70**	AM13	IO	SSTL
P0D71	AK13	IO	SSTL	**P0D72**	AN14	IO	SSTL	**P0D73**	AL14	IO	SSTL
P0D74	AJ14	IO	SSTL	**P0D75**	AP15	IO	SSTL	**P0D76**	AK15	IO	SSTL
P0D77	AN16	IO	SSTL	**P0D78**	AL16	IO	SSTL	**P0D79**	AJ16	IO	SSTL
P0D7CK	AJ10	IO	SSTL	**P0D8**	P1	IO	SSTL	**P0D9**	P3	IO	SSTL
P0S0	AM9	IO	SSTL	**P0S1**	R4	IO	SSTL	**P0S2**	V3	IO	SSTL
P0S3	AA4	IO	SSTL	**P0S4**	AD3	IO	SSTL	**P0S5**	AG4	IO	SSTL
P0S6	AL6	IO	SSTL	**P0S7**	AM3	IO	SSTL	**P0S8**	AL12	IO	SSTL
P0S9	AM15	IO	SSTL	**P0VREF0**	AH12	I	ANALOG	**P0VREF1**	T7	I	ANALOG
P0VREF2	W7	I	ANALOG	**P0VREF3**	AB7	I	ANALOG	**P0VREF4**	AE7	I	ANALOG
P0VREF5	AG7	I	ANALOG	**P0VREF6**	AH11	I	ANALOG	**P0VREF7**	AH9	I	ANALOG
P0VREF8	AH14	I	ANALOG	**P0VREF9**	AH15	I	ANALOG				

Table 22 Bridge port 0 signals

Signal	Pin	Dir	Type	Signal	Pin	Dir	Type	Signal	Pin	Dir	Type
AVDD6	AE22	I	ANALOG	**AVSS6**	AD22	I	ANALOG	**P1D0CK**	AN27	IO	SSTL
P1D1	AL27	IO	SSTL	**P1D10**	P30	IO	SSTL	**P1D11**	R33	IO	SSTL
P1D12	R29	IO	SSTL	**P1D13**	T34	IO	SSTL	**P1D14**	T32	IO	SSTL
P1D15	T30	IO	SSTL	**P1D16**	U33	IO	SSTL	**P1D17**	U31	IO	SSTL
P1D18	U29	IO	SSTL	**P1D19**	V34	IO	SSTL	**P1D2**	AJ27	IO	SSTL
P1D20	V30	IO	SSTL	**P1D21**	W33	IO	SSTL	**P1D22**	W31	IO	SSTL
P1D23	W29	IO	SSTL	**P1D24**	Y34	IO	SSTL	**P1D25**	Y32	IO	SSTL
P1D26	Y30	IO	SSTL	**P1D27**	AA33	IO	SSTL	**P1D28**	AA29	IO	SSTL
P1D29	AB34	IO	SSTL	**P1D3**	AP26	IO	SSTL	**P1D30**	AB32	IO	SSTL
P1D31	AB30	IO	SSTL	**P1D32**	AC33	IO	SSTL	**P1D33**	AC31	IO	SSTL
P1D34	AC29	IO	SSTL	**P1D35**	AD34	IO	SSTL	**P1D36**	AD30	IO	SSTL
P1D37	AE33	IO	SSTL	**P1D38**	AE31	IO	SSTL	**P1D39**	AE29	IO	SSTL
P1D4	AK26	IO	SSTL	**P1D40**	AF34	IO	SSTL	**P1D41**	AF32	IO	SSTL
P1D42	AF30	IO	SSTL	**P1D43**	AG33	IO	SSTL	**P1D44**	AG29	IO	SSTL
P1D45	AH34	IO	SSTL	**P1D46**	AH32	IO	SSTL	**P1D47**	AH30	IO	SSTL
P1D48	AP30	IO	SSTL	**P1D49**	AM30	IO	SSTL	**P1D5**	AN25	IO	SSTL
P1D50	AK30	IO	SSTL	**P1D51**	AN29	IO	SSTL	**P1D52**	AJ29	IO	SSTL
P1D53	AP28	IO	SSTL	**P1D54**	AM28	IO	SSTL	**P1D55**	AK28	IO	SSTL
P1D56	AN33	IO	SSTL	**P1D57**	AL33	IO	SSTL	**P1D58**	AJ33	IO	SSTL
P1D59	AP32	IO	SSTL	**P1D6**	AL25	IO	SSTL	**P1D60**	AK32	IO	SSTL
P1D61	AN31	IO	SSTL	**P1D62**	AL31	IO	SSTL	**P1D63**	AJ31	IO	SSTL
P1D64	AP24	IO	SSTL	**P1D65**	AM24	IO	SSTL	**P1D66**	AK24	IO	SSTL
P1D67	AN23	IO	SSTL	**P1D68**	AJ23	IO	SSTL	**P1D69**	AP22	IO	SSTL
P1D70	AM22	IO	SSTL	**P1D71**	AK22	IO	SSTL	**P1D72**	AN21	IO	SSTL
P1D73	AL21	IO	SSTL	**P1D74**	AJ21	IO	SSTL	**P1D75**	AP20	IO	SSTL

Table 23 Bridge port 1 signals

This information applies to a product under development.
Specifications and characteristics are subject to change without notice.

Signal	Pin	Dir	Type	Signal	Pin	Dir	Type	Signal	Pin	Dir	Type
P1D76	AK20	IO	SSTL	**P1D77**	AN19	IO	SSTL	**P1D78**	AL19	IO	SSTL
P1D79	AJ19	IO	SSTL	**P1D7CK**	AJ25	IO	SSTL	**P1D8**	P34	IO	SSTL
P1D9	P32	IO	SSTL	**P1S0**	AM26	IO	SSTL	**P1S1**	R31	IO	SSTL
P1S2	V32	IO	SSTL	**P1S3**	AA31	IO	SSTL	**P1S4**	AD32	IO	SSTL
P1S5	AG31	IO	SSTL	**P1S6**	AL29	IO	SSTL	**P1S7**	AM32	IO	SSTL
P1S8	AL23	IO	SSTL	**P1S9**	AM20	IO	SSTL	**P1VREF0**	AH23	I	ANALOG
P1VREF1	P28	I	ANALOG	**P1VREF2**	V28	I	ANALOG	**P1VREF3**	Y28	I	ANALOG
P1VREF4	AD28	I	ANALOG	**P1VREF5**	AF28	I	ANALOG	**P1VREF6**	AH24	I	ANALOG
P1VREF7	AH26	I	ANALOG	**P1VREF8**	AH21	I	ANALOG	**P1VREF9**	AH20	I	ANALOG

Table 23 Bridge port 1 signals

Signal	Pin	Dir	Type	Signal	Pin	Dir	Type
HCLK	J28	I	HSTL	**HERR**	M30	OD	HSTL
HGNT	J30	I	HSTL	**HIRQ_N**	N29	OD	HSTL
HREQ	K30	O	HSTL	**HRXD0**	L34	I	HSTL
HRXD1	L33	I	HSTL	**HRXD2**	M34	I	HSTL
HRXD3	M33	I	HSTL	**HRXD4**	N33	I	HSTL
HRXD5	M32	I	HSTL	**HRXD6**	L31	I	HSTL
HRXD7	N31	I	HSTL	**HRXEOP**	L29	I	HSTL
HRXSTP	L30	OD	HSTL	**HRXVAL**	M31	I	HSTL
HTXD0	H34	OT	HSTL	**HTXD1**	H33	OT	HSTL
HTXD2	J34	OT	HSTL	**HTXD3**	K34	OT	HSTL
HTXD4	K33	OT	HSTL	**HTXD5**	J32	OT	HSTL
HTXD6	H31	OT	HSTL	**HTXD7**	K31	OT	HSTL
HTXEOP	H29	OT	HSTL	**HTXSTP**	H30	I	HSTL
HTXVAL	K29	IO	HSTL	**HVREF**	M28	I	ANALOG

Table 24 Host debug port signals

Signal	Pin	Dir	Type	Signal	Pin	Dir	Type	Signal	Pin	Dir	Type
MA0	D18	O	SSTL	**MA1**	C17	O	SSTL	**MA10**	D20	O	SSTL
MA11	F12	O	SSTL	**MA12**	F11	O	SSTL	**MA13**	F24	O	SSTL
MA14	F8	O	SSTL	**MA2**	D17	O	SSTL	**MA3**	F17	O	SSTL
MA4	F16	O	SSTL	**MA5**	E16	O	SSTL	**MA6**	E14	O	SSTL
MA7	E13	O	SSTL	**MA8**	D14	O	SSTL	**MA9**	E11	O	SSTL
MBA0	F21	O	SSTL	**MBA1**	F20	O	SSTL	**MBA2**	E8	O	SSTL
MCAS_N	D23	O	SSTL	**MCB0**	A18	IO	SSTL	**MCB1**	C18	IO	SSTL
MCB2	B21	IO	SSTL	**MCB3**	A21	IO	SSTL	**MCB4**	F18	IO	SSTL
MCB5	E18	IO	SSTL	**MCB6**	B19	IO	SSTL	**MCB7**	A20	IO	SSTL
MCK0_N	A16	O	SSTL	**MCK0_P**	B16	O	SSTL	**MCK1_N**	A6	O	SSTL
MCK1_P	B6	O	SSTL	**MCK2_N**	B30	O	SSTL	**MCK2_P**	A30	O	SSTL
MCK3_N	A15	O	SSTL	**MCK3_P**	B15	O	SSTL	**MCK4_N**	A5	O	SSTL
MCK4_P	B5	O	SSTL	**MCK5_N**	B31	O	SSTL	**MCK5_P**	A31	O	SSTL
MCK6_N	G34	O	SSTL	**MCK6_P**	F34	O	SSTL	**MCKE**	F6	O	SSTL
MDM0	F3	O	SSTL	**MDM1**	D6	O	SSTL	**MDM2**	C10	O	SSTL
MDM3	B14	O	SSTL	**MDM4**	A23	O	SSTL	**MDM5**	C27	O	SSTL

Table 25 Local memory interface signals

This information applies to a product under development.
Specifications and characteristics are subject to change without notice.

Signal	Pin	Dir	Type	Signal	Pin	Dir	Type	Signal	Pin	Dir	Type
MDM6	A33	O	SSTL	**MDM7**	F33	O	SSTL	**MDM8**	E19	O	SSTL
MDQ0	E4	IO	SSTL	**MDQ1**	E1	IO	SSTL	**MDQ10**	C8	IO	SSTL
MDQ11	E10	IO	SSTL	**MDQ12**	A3	IO	SSTL	**MDQ13**	C4	IO	SSTL
MDQ14	A7	IO	SSTL	**MDQ15**	D8	IO	SSTL	**MDQ16**	D9	IO	SSTL
MDQ17	A9	IO	SSTL	**MDQ18**	D12	IO	SSTL	**MDQ19**	D15	IO	SSTL
MDQ2	C2	IO	SSTL	**MDQ20**	B8	IO	SSTL	**MDQ21**	A8	IO	SSTL
MDQ22	D11	IO	SSTL	**MDQ23**	C11	IO	SSTL	**MDQ24**	A12	IO	SSTL
MDQ25	B12	IO	SSTL	**MDQ26**	F15	IO	SSTL	**MDQ27**	C16	IO	SSTL
MDQ28	A11	IO	SSTL	**MDQ29**	B11	IO	SSTL	**MDQ3**	B3	IO	SSTL
MDQ30	A14	IO	SSTL	**MDQ31**	C14	IO	SSTL	**MDQ32**	B22	IO	SSTL
MDQ33	C22	IO	SSTL	**MDQ34**	B25	IO	SSTL	**MDQ35**	A26	IO	SSTL
MDQ36	C21	IO	SSTL	**MDQ37**	A22	IO	SSTL	**MDQ38**	C24	IO	SSTL
MDQ39	A25	IO	SSTL	**MDQ4**	F5	IO	SSTL	**MDQ40**	D26	IO	SSTL
MDQ41	A27	IO	SSTL	**MDQ42**	C28	IO	SSTL	**MDQ43**	A29	IO	SSTL
MDQ44	D24	IO	SSTL	**MDQ45**	C25	IO	SSTL	**MDQ46**	A28	IO	SSTL
MDQ47	B28	IO	SSTL	**MDQ48**	D30	IO	SSTL	**MDQ49**	C31	IO	SSTL
MDQ5	F1	IO	SSTL	**MDQ50**	C32	IO	SSTL	**MDQ51**	D32	IO	SSTL
MDQ52	D29	IO	SSTL	**MDQ53**	C30	IO	SSTL	**MDQ54**	C34	IO	SSTL
MDQ55	C33	IO	SSTL	**MDQ56**	E31	IO	SSTL	**MDQ57**	E33	IO	SSTL
MDQ58	F28	IO	SSTL	**MDQ59**	G32	IO	SSTL	**MDQ6**	D3	IO	SSTL
MDQ60	E30	IO	SSTL	**MDQ61**	D34	IO	SSTL	**MDQ62**	F32	IO	SSTL
MDQ63	F29	IO	SSTL	**MDQ7**	C1	IO	SSTL	**MDQ8**	A4	IO	SSTL
MDQ9	D5	IO	SSTL	**MDQS0**	D1	IO	SSTL	**MDQS1**	C7	IO	SSTL
MDQS2	A10	IO	SSTL	**MDQS3**	C13	IO	SSTL	**MDQS4**	B24	IO	SSTL
MDQS5	D27	IO	SSTL	**MDQS6**	B33	IO	SSTL	**MDQS7**	F30	IO	SSTL
MDQS8	A19	IO	SSTL	**MDSG0**	E2	IO	SSTL	**MDSG1**	C5	IO	SSTL
MDSG2	B9	IO	SSTL	**MDSG3**	A13	IO	SSTL	**MDSG4**	A24	IO	SSTL
MDSG5	B27	IO	SSTL	**MDSG6**	A32	IO	SSTL	**MDSG7**	E34	IO	SSTL
MDSG8	C19	IO	SSTL	**MODT0**	E21	O	SSTL	**MODT1**	E25	O	SSTL
MODT2	E27	O	SSTL	**MODT3**	E28	O	SSTL	**MRAS_N**	D21	O	SSTL
MS0_N	F19	O	SSTL	**MS1_N**	F23	O	SSTL	**MS2_N**	E24	O	SSTL
MS3_N	F26	O	SSTL	**MVREF0**	G10	I	ANALOG	**MVREF1**	G11	I	ANALOG
MVREF2	G13	I	ANALOG	**MVREF3**	G14	I	ANALOG	**MVREF4**	G21	I	ANALOG
MVREF5	G22	I	ANALOG	**MVREF6**	G24	I	ANALOG	**MVREF7**	G25	I	ANALOG
MVREF8	G17	I	ANALOG	**MVREF9**	G16	I	ANALOG	**MWE_N**	E22	O	SSTL

Table 25 Local memory interface signals

Signal	Pin	Dir	Type	Signal	Pin	Dir	Type
AVDD1	R10	I	ANALOG	**AVDD2**	T10	I	ANALOG
AVSS1	R11	I	ANALOG	**AVSS2**	T11	I	ANALOG
CKIN_N	K1	I	SSTL	**CKIN_P**	J1	I	SSTL
CNFG0	G4	I	LVCMOS	**CNFG1**	H4	I	LVCMOS
CNFG10	L5	I	LVCMOS	**CNFG11**	M5	I	LVCMOS
CNFG2	J4	I	LVCMOS	**CNFG3**	K4	I	LVCMOS

Table 26 System services signals

PRELIMINARY TECHNICAL DATA

Signal	Pin	Dir	Type	Signal	Pin	Dir	Type
CNFG4	L4	I	LVCMOS	**CNFG5**	M4	I	LVCMOS
CNFG6	N4	I	LVCMOS	**CNFG7**	H5	I	LVCMOS
CNFG8	J5	I	LVCMOS	**CNFG9**	K5	I	LVCMOS
RST_N	G1	I	LVCMOS	**THDN**	L7	IO	ANALOG
THDP	K7	IO	ANALOG				

Table 26 System services signals

Signal	Pin	Dir	Type	Signal	Pin	Dir	Type
TCK	M1	I	LVCMOS	**TDI**	M2	I	LVCMOS
TDO	N2	O	LVCMOS	**TMS**	N1	I	LVCMOS
TRST_N	M3	I	LVCMOS				

Table 27 Test signals

To assist with planning board layout, Figure 20 shows the approximate location of functional groups of pins and the position of the power and clock pins.

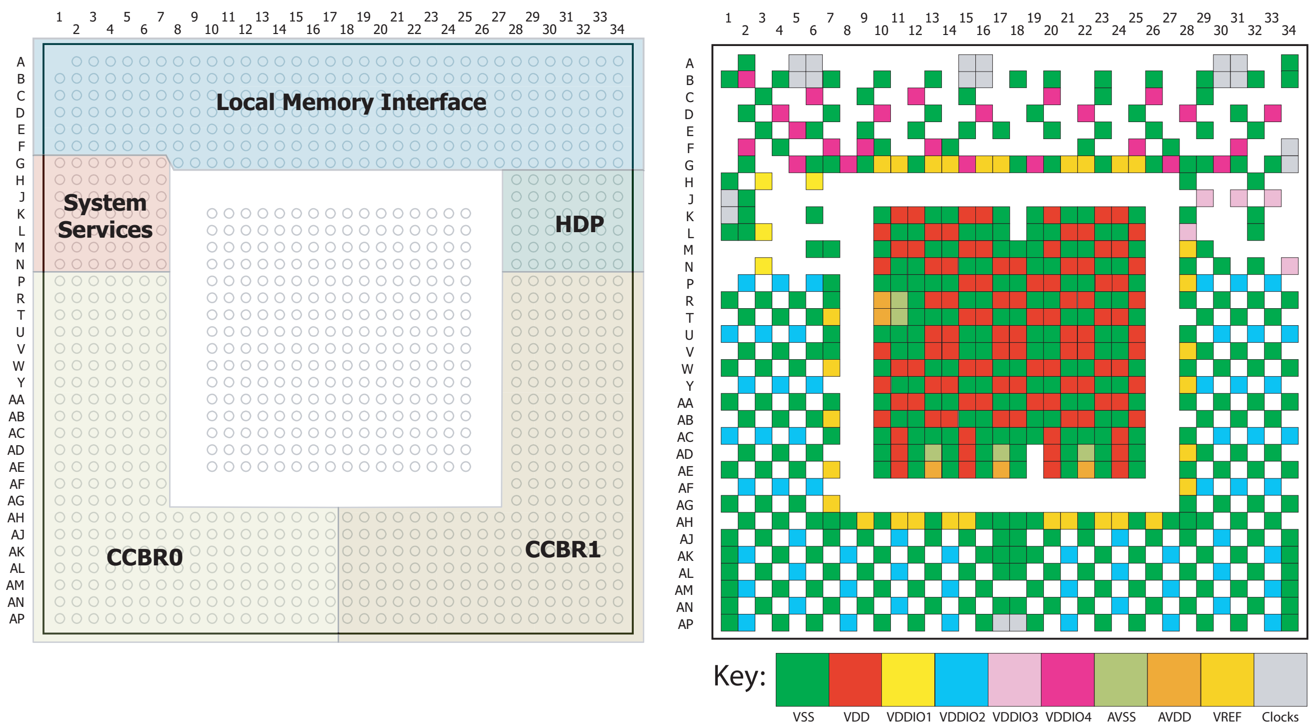

Figure 20 Signal location guide: functions and power (PCB view)

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PRELIMINARY TECHNICAL DATA

Ordering information

The available products are shown in the table below. These are the products planned for volume production. Contact your ClearSpeed representative to confirm availability of specific products and to check on new releases.

ClearSpeed order code	Device marking	Description
	CSX600-C0CB-ES	Engineering samples. Uncharacterized.
		Engineering samples. Uncharacterized.

The device marking is made up of the following elements.

CSX600 – A 0 C B e1 – ES

Product

Revision

Speed Grade

0 = ungraded

Temperature Range

C = Commercial (0°C to 70°C)

Package Type

B = Ball Grid Array (BGA)

JEDEC E-Cat Code

blank = Not Pb free

e1 = SnAgCu

Engineering Sample

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